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THESIS

OPTICAL SNS FOLDING CIRCUIT DESIGN

by

Craig A. Crowe

March 1995

Thesis Advisor:	Phillip E. Pace
Co-Advisor:	Ron J. Pieper

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Recently, a new technique has been described for extending the resolution of an integrated optical multi-interferometer analog-to-digital converter (ADC). These types of ADCs can directly digitize the signals from an antenna and play an important role in eliminating the need for intermediate frequency and baseband processing. With resolution greater than 12 bits, these types of architectures are useful for a variety of applications. The new technique is based on the incorporation of a symmetrical number system (SNS) encoding to provide high resolution (greater than 1-bit per interferometer) while also reducing the complexity of the optical hardware. In this thesis the optical processor for an 8-bit folding ADC is designed. LabVIEW simulation of the interferometers is used to simultaneously allow for the testing of the digital circuit boards and the development of the optical front end of the ADC. Each component considered for the 8-bit optical design is discussed and the reason for the component selection is given. The 8-bit optical design is then documented and tested.

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OPTICAL SNS FOLDING CIRCUIT DESIGN

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ABSTRACT

Recently, a new technique has been described for extending the resolution of an integrated optical multi-interferometer analog-to-digital converter (ADC). These types of ADCs can directly digitize the signals from an antenna and play an important role in eliminating the need for intermediate frequency and baseband processing. With resolution greater than 12 bits, these types of architectures are useful for a variety of applications. The new technique is based on the incorporation of a symmetrical number system (SNS) encoding to provide high resolution (greater than 1-bit per interferometer) while also reducing the complexity of the optical hardware. In this thesis the optical processor for an 8-bit folding ADC is designed. LabVIEW simulation of the interferometers is used to simultaneously allow for the testing of the digital circuit boards and the development of the optical front end of the ADC. Each component considered for the 8-bit optical design is discussed and the reason for the component selection is given. The 8-bit optical design is then documented and tested.

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I. INTRODUCTION

A. INTEGRATED OPTICAL SYMMETRICAL NUMBER SYSTEM SIGNAL PROCESSING

1. Integrated Optical SNS ADC

The most efficient (sampling) ADCs demonstrated to date use integrated electro-optical guided-wave technology (in lithium niobate, gallium arsenide, or indium phosphide). Symmetrical folding of the input signal is realized with Mach-Zhender interferometric (MZI) waveguide modulators arranged in a parallel configuration [Ref. 1-5]. These modulators use the linear Pockels effect and provide a convenient method for coupling a wideband electrical signal into an optical processing system through the modulator electrodes.

Recently, a technique that extends the resolution of an integrated optical multi-interferometer analog-to-digital converter was described [Ref. 2,6]. The optical output waveform for each interferometer is symmetrically folded at twice a proper modulus. A small comparator ladder mid-level quantizes each interferometer's detected output to encode the analog signal in a symmetrical number system (SNS) format. By incorporating the SNS encoding, resolution greater than 1-bit per interferometer can be provided.

The SNS is composed of a number of pairwise relatively prime (PRP) moduli m_i. The integers within each SNS modulus are representative of a symmetrically folded waveform with the period of the waveform equal to twice the PRP modulus. For m given, the integer values within twice the individual modulus are given by:

$$x_m = [0, 1, \ldots, m-1, m-1, \ldots, 1, 0]. \qquad (1)$$

The SNS folding waveform is symmetrical about the midpoint and is compatible with other folding waveforms. Due to the presence of ambiguities, the integers within equation (1) do not form a complete system of length $2m$ by themselves. It is well known however, that the inclusion of additional redundant moduli can effectively detect and correct errors within a residue number system (RNS) representation of a number. The SNS formulation is based on a similar concept which allows the ambiguities to occur. The ambiguities that arise within the SNS are resolved by using various arrangements of the SNS moduli. By considering the derived moduli arrangements, the SNS is rendered a complete system having a one-to-one correspondence with the RNS. For N equal to the number of PRP moduli, the dynamic range M of the system is [Ref. 2]

$$M=\prod_{i=1}^{N} m_i . \tag{2}$$

The SNS can serve as a source for resolution enhancement in an ADC by decomposing the analog amplitude analyzing function into a number of parallel sub-operations (moduli) that are of smaller computational complexity. Each sub-operation for a different modulus requires only a precision in accordance with that modulus. A much higher resolution is achieved after the results of these low precision sub-operations are recombined. That is, the resolution of each interferometer is greater than 1 bit per interferometer. The input signal is folded in parallel with each folding period equal to twice a particular modulus. The folded waveform at the output of each folding circuit is mid-level quantized with a small comparator ladder to encode the input signal in the SNS format. An encoder then converts the SNS representation to a more familiar digital output such as a binary representation. With the SNS encoding any combination of folding periods and comparator arrangements can be analyzed exactly.

The optical output power from a single guided-wave interferometer is symmetrical and periodic and can thus be used to implement each folding circuit (modulus) in the SNS ADC. Figure 1 shows a block diagram of the SNS ADC which uses three interferometers. The interferometer normalized output is a function of both the sampled analog voltage v and the modulus m_i as

$$I(v,m)=\cos^2\left(\frac{\pi v}{2m_i}+\frac{\pi}{2}\right). \tag{3}$$

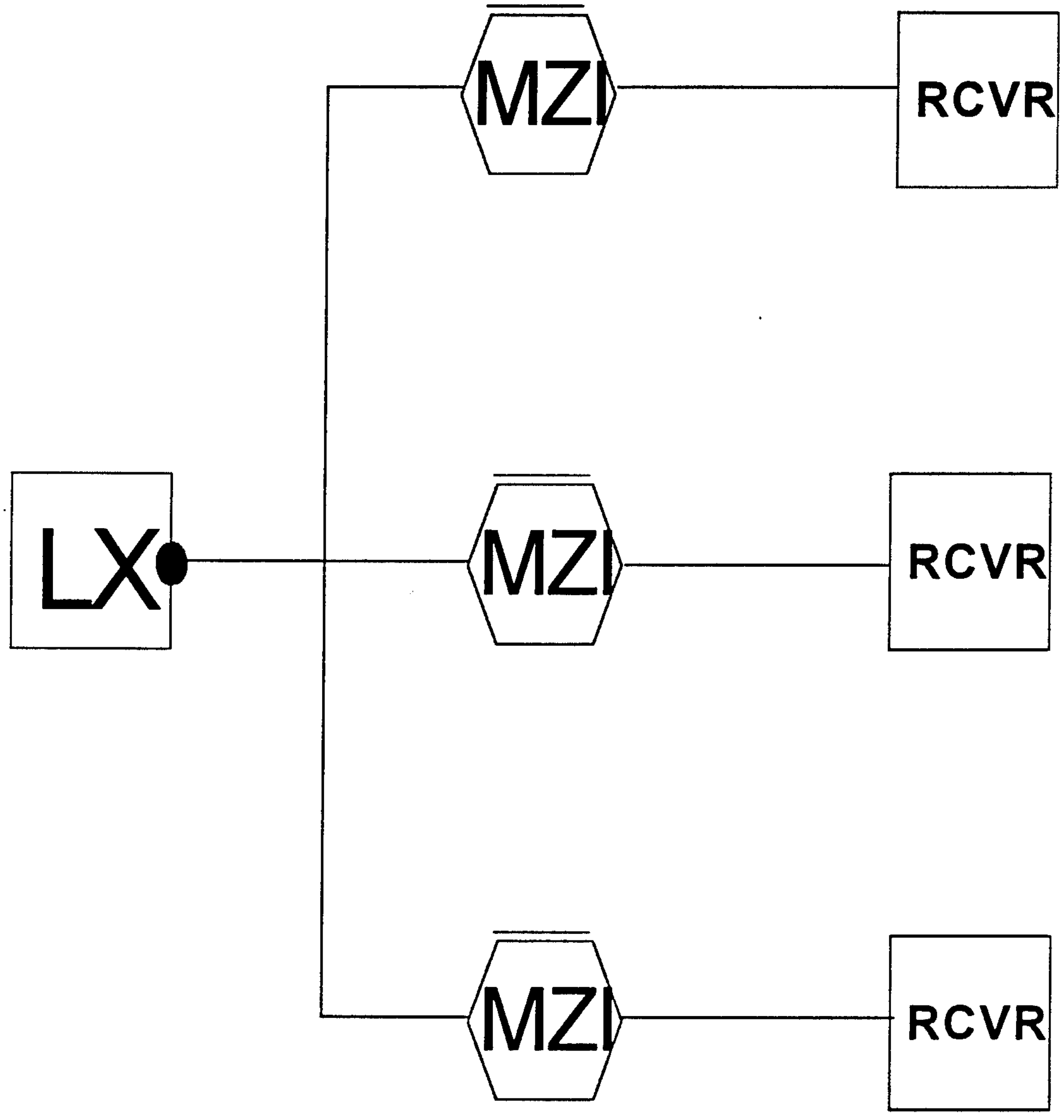


Figure 1. SNS ADC Block Diagram With Three Interferometers

That is, the voltage dependent phase shift $\Delta\phi_i = \frac{\pi v}{2m_i}$. In terms of the electro-optical parameters

$$\Delta\phi_i = \mathrm{KL_i}v \tag{4}$$

where $\mathrm{L_i}$ is the length of the electrode and K is a constant that depends on the index of refraction, the electro-optic coefficient, the interelectrode gap, the electrical-optical overlap parameter, and the optical wavelength. Thus, the electrode lengths vary as

$$\mathrm{L_i} = \frac{\pi}{\mathrm{K}m_i} \tag{5}$$

or inversely proportional to m_i. Since the moduli are PRP and can be chosen to be similar in magnitude, the electrode lengths are similar in size. The advantage here is that the interferometers (folding circuits) in the system can be identical devices. The small electrode length difference that is required for each modulus, can be instrumented by placing a small attenuator at the analog input.

The folding circuit for each modulus requires $m_i - 1$ comparators at the output of the detector. With the waveform given by equation (3), the normalized threshold values for the comparators within each modulus m_i are

$$T_{i,j} = \cos^2\left(\frac{\pi v_j}{2m_i} + \frac{\pi}{2}\right) \tag{6}$$

where

$$v_j \in \{1, 2, 3, \ldots, m_i - 1\}. \tag{7}$$

That is, the comparator thresholds are tailored to the interferometer output waveform. The size of the least significant bit (LSB) for the SNS ADC is

$$\mathrm{V_{LSB}} = \frac{\mathrm{V}_\pi}{m_{\min}}. \tag{8}$$

where $m_{\min}$ is the smallest modulus and V_π is the amount of electrode voltage needed to transition the normalized output from a minimum ($\Delta\phi$=0) to a maximum ($\Delta\phi$=π).

The SNS ADC employs integrated optical interferometers to preprocess the analog signal. Each interferometer folds the input signal at a particular PRP modulus m_i and a small comparator ladder is used after each detector to detect the various voltage levels and encode the input signal into the SNS format. The normalized interferometer output can be expressed as

$$I = \tfrac{1}{2} + \tfrac{1}{2}\cos\left[\Delta\phi(\nu) + \pi\right]. \tag{9}$$

The voltage dependent phase shift $\Delta\phi(\nu)$ for a push-pull electrode configuration can be expressed in terms of the electro-optic parameters as

$$\Delta\phi(\nu) = \frac{2\pi n_e^3 \Gamma L_i \nu r}{G\lambda}, \tag{10}$$

where n_e is the effective index of the optical guide, r is the pertinent electro-optic coefficient, G is the interelectrode gap, Γ is the electrical-optical overlap parameter, and λ is the free-space optical wavelength. V_π in terms of the electro-optical parameters is

$$V_\pi = \frac{G\lambda}{2L_i n_e^3 r\Gamma}. \tag{11}$$

Another device constraint is the maximum voltage that may be applied to the electrodes. Applied voltage beyond the rated maximum (minimum) will spark across the electrode structure and damage the device. The specifications of V_π and v_{max} reveal the maximum number of folds available from the device. A complete fold is $2V_\pi$. The maximum number of folds F available from a device is therefore

$$F = \frac{2v_{max}}{2V_\pi}. \tag{12}$$

The smallest modulus within the SNS system requires the largest number of folds to instrument the dynamic range M . Since a complete fold is $2V_\pi = 2m_i$, the largest number of folds required from an interferometer in a B-bit SNS ADC is

$$F_{req} = \frac{2^B - 1}{2m_{min}} < \frac{v_{max}}{V_\pi}, \qquad (13)$$

where m_{min} is the smallest modulus in the SNS system.

2. 8-bit SNS ADC Design

The 8-bit SNS ADC uses a sampling frequency f_s=5MHz and contains three parallel channels. The three interferometers being used were built by the Naval Research Laboratory and are on loan from the National Security Agency. The maximum voltage that can be applied to these devices is approximately v_{max} = 30volts. The V_π is approximately 2.1 volts (minimum modulus). The total number of folds available from each device is approximately 14. Using equation (13), the minimum modulus is calculated as $m_{min} = 9$. Since the channel moduli must be pair-wise relatively prime the remaining two channels are $m_2 = 10$ and $m_3 = 11$. From equation (8), the size of the LSB is 233 mV. Including the few additional comparators for error decimation, the total number of comparators required is 37, with a maximum of 18 loaded in parallel.

B. PRINCIPAL CONTRIBUTIONS

In this thesis, an 8-bit optical SNS folding circuit is designed as a front end to the digital processor. LabVIEW simulation of the interferometers is used to simultaneously allow the testing of the digital processor and the development of the optical front end of the ADC. Each component considered for the 8-bit optical design is discussed and the reason for component selection is detailed. Phasing and biasing of each optical folding circuit is reviewed and a link budget analysis is given. The 8-bit optical design is then documented and tested.

C. THESIS OUTLINE

Chapter II of this thesis consists of an overview of LabVIEW followed by a description of the initial development of LabVIEW VIs. Next, the extended development of LabVIEW VIs is discussed. Finally, the characteristic waveforms for each interferometer device are obtained with LabVIEW and documented. Chapter III provides the detailed description of the components considered and selected for the final optical design. The general characteristics of each interferometer device are also detailed. The characteristic waveforms are again obtained but this time with the RTD720A Real Time Digitizer. Single-mode fiber and connectors are discussed with a discussion on Brillouin and Raman Scattering. Finally, the peculiarities of polarization maintaining fiber and polarization maintaining connectors as they apply to the design are detailed. Chapter IV discusses the final 8-bit design and provides the results of initial testing and evaluation. Following the summary of Chapter V, Appendix A provides the design methods used to create the LabVIEW VIs for this research. The LabVIEW graphical source code is also provided for the collection of LabVIEW VIs developed in this research. Appendix B gives the Matlab programming language source code for the programs MACH1.M and STR.M. MACH1.M analyzes the LabVIEW output and plots the interferometer characteristic waveforms. STR.M plots a staircase used in Chapter IV to illustrate the comparator ladder.

II. IDEAL INTERFEROMETER WAVEFORM GENERATION

A. OVERVIEW OF LABVIEW

LabVIEW is a graphical programming development application, similar to a C or Basic programming development system. Whereas other development systems utilize text-based languages to produce lines of code, LabVIEW relies on a graphical interface to produce programs in a block diagram format.

Although the LabVIEW manuals state that "little" programming experience is necessary to use LabVIEW, a basic understanding of programming methodology is helpful. LabVIEW takes advantage of terms, icons, and ideas which scientists and engineers will find familiar. LabVIEW relies on graphical symbols and icons to enable programming actions.

LabVIEW includes function and subroutine libraries that can be used for the majority of programming applications. Within LabVIEW there are also application libraries which can be used directly or modified to fit the user's need for data acquisition, external instrument control, data analysis, and data presentation and storage. LabVIEW also includes program development tools that allow the user to easily develop and debug a program.[Ref. 7]

B. INITIAL DEVELOPMENT OF LABVIEW VI'S

1. Initial Efforts

The design of the 8-bit system requires the simultaneous development and testing of the circuit boards and optical system development. This means that there will be a delay in getting the necessary output from the Mach-Zhender interferometers while the optical system is under development. Consequently a simulation of the interferometer Modulus 9, Modulus 10, and Modulus 11 output is necessary to allow the testing and development of the circuit boards.

The goal of the initial effort is to simulate the folded output of the Modulus 9, Modulus 10, and Modulus 11 interferometers to allow circuit verification. For a interferometer device with a particular V_π and V_{max} the maximum number of folds is determined by

$$(\text{no. folds})_{max} \leq \frac{V_{max}}{V_\pi}. \tag{14}$$

In the 8-bit design $2V_\pi = 4.507V$ with $V_{max} = 30V$. The number of folds for Modulus 9 are

$$(\text{no. folds})_9 \leq \frac{2(30)}{4.507} = 13.313. \tag{15}$$

The number of folds for Modulus 10 and Modulus 11 are computed from a ratio of the lowest modulus to the modulus of interest. The number of folds for Modulus 10 and Modulus 11 are

$$(\text{no. folds})_{10} \leq (\text{no. folds})_9 \times \frac{9}{10} \tag{16}$$

$$(\text{no. folds})_{11} \leq (\text{no. folds})_9 \times \frac{9}{11}. \tag{17}$$

These ratios are used in the generation of the simulated waveforms for the three moduli.

The actual output of an interferometer is a raised $(\text{cosine})^2$ wave. Using trigonometric identities a $(\text{cosine})^2$ wave becomes a cosine wave with a DC offset

$$\cos^2 x = \tfrac{1}{2}(1 + \cos 2x). \tag{18}$$

The programs initially developed use a sine waveform with a DC offset and a phase shift of 270° to simulate the moduli folded waveforms. In order to output the waveforms to the circuit boards, three AT-MIO-16F-5 data acquisition cards are installed in an IBM compatible 486 DX-2 computer. Three cards are necessary to output three analog waveforms having different frequencies. The circuit boards are connected to LabVIEW through adapters which connect to the AT-MIO-16F-5 data acquisition cards.

The file, JEFFSTEP.VI, produces three equal length arrays allowing the user to input the 'Number of generation points' that are required. The frequency ratios are calculated from the cycles ratio for each folded output waveform. For this specific case the number of cycles produced are 110, 99, and 90 corresponding to the Modulus 9, Modulus 10, and Modulus 11 respectively. The front panel is designed to allow the user to vary the amplitude, DC offset, number of cycles to produce, and which array index to output. The front panel also displays each of the folded outputs, the output voltage of each channel, and the number of generation points for observation. The number of generation points is found by

$$\text{Number of points} = \frac{\text{Number of generation points}}{\text{lowest modulus cycles}} \times \text{Number of Cycles}. \qquad (19)$$

When the program is run the output is generated for the selected index. The output voltage is held until the index is reset and the program is run again. The step size is the incremental voltage change for each output waveform that is produced when the index is incremented. The step size in volts for each folded waveform is determined by [Ref. 8]

$$\text{Step size} = 5\ \text{Volts} \div \left(\frac{\text{Number of generation points}}{\text{Number of modulus cycles}} \times 0.5\right) \qquad (20)$$

2. VI Enhancement Goals

To continue with the simultaneous development of the ADC circuit boards and optical processor, the programs created in the initial efforts need to be enhanced to provide the following features:

1. Output the array data to an output file for analysis and printing.
2. Automate the system to provide array output from start to finish without having to manually index the array.
3. Provide an external trigger to automate data collection at the HP1631D Logic Analyzer.

4. Provide a voltage ramp output to drive one Mach-Zhender interferometer.
5. Collect the word data (ie. eight bits from the word + 1 bit parity) from the Analog-to-Digital Converter within LabVIEW for analysis and printing. This step automates the data collection.

C. EXTENDED DEVELOPMENT OF LABVIEW VI'S

The enhancement of the initial programs started by renaming a copy of JEFFSTEP.VI, to CRAIG.VI. From this file the design is done in increments from CRAIG.VI through CRAIG8.VI. Each successive design attempts to add a new feature to the VI. Each new file is tested and evaluated and the design process repeats.

1. Array Data Output and Automation

Files with names CRAIG1.VI through CRAIG3.VI experiment with different possible designs to automate the output of the array. CRAIG4.VI is the result. This VI automates the array output so that the array index no longer has to be manually advanced at the control panel. The voltages are set to change within the for loop every one second. The voltage outputs are supplied to the Modulus 9, Modulus 10, and Modulus 11 boards at DAC0 out, pin number 20. In addition , in CRAIG4.VI, the array output is written to a spreadsheet file in ASCII text format for later analysis and printing. The array output file is named OUTPUT.TXT. For a more detailed discussion of this development with the corresponding figures refer to Appendix A.

2. External Trigger

The next step of the design involves the HP1631D Logic Analyzer. The data for each run can be acquired with the HP1631D Logic Analyzer if LabVIEW can generate an external trigger. Using the write to digital line VI in LabVIEW, a loop is designed to drive the output pin on the Modulus 9 board, pin number 25 high then low. The trigger loop is within the array loop (a nested loop structure). The array loop executes every one second setting the voltages at the Modulus 9, Modulus 10, and Modulus 11 boards. The nested trigger loop executes 0.5 seconds later driving pin 25 high then low. The HP1631D Logic Analyzer is set to trigger on the negative edge of the pulse. The output on pin 25 is a square wave, but appears very noisy. This has to be corrected in the following designs.

In CRAIG5.VI the noisy trigger output is addressed. A pulse pattern VI replaces the write to digital line VI. This VI generates a pulse with a set amplitude and width. Again the output is on the Modulus 9 board, pin 25. The pulse pattern VI is less reliable and more noisy than using the write to digital line VI as done previously in CRAIG4.VI. This is not a viable solution to the trigger problem.

In CRAIG6.VI the noisy trigger output is again addressed. A nested sequence structure replaces the nested trigger loop. The array voltage loop is set to execute every second. The sequence structure executes after the waveform voltages within the loop are set to their respective values. The number "0" sequence contains a wait 250 ms (1/4 second) timer. The number "1" sequence executes next. It contains the write to digital line VI driving the output on pin 25 high. The number "2" sequence follows. It contains a wait 250 ms timer. The number "3" sequence is executed next. It contains the write to digital line VI driving the output on pin 25 low this time. The time of the rising and falling edges of the trigger are adjusted by adjusting the timers in sequence "0" and sequence "2". Note: The trigger must execute within the timing of the loop ie., if the loop executes every one second, the entire time for the trigger cannot exceed one second.

This design for the trigger is clean and reliable. For a more detailed discussion of this development with the corresponding figures refer to Appendix A.

3. Voltage Ramp Output

Next, it is necessary to obtain the transfer functions for each of the three NRL Mach- Zhender interferometers. This requires a voltage ramp output from LabVIEW. This is addressed in CRAIG7.VI.

In CRAIG7.VI a loop containing a formula node is added to the system. This loop is outside of the array voltage output loop. The formula node loop generates a normalized ramp voltage with the same number of voltage points for the interferometer input as the voltage outputs coming from the Modulus 9, Modulus 10, and Modulus 11 boards simulating the folds of the interferometer. The formula within the formula node is given as

$$y = \frac{x}{45.5 \times 69.677} \times 2V_\pi \tag{21}$$

where $V_\pi = 2.45$V, and x is the point number. The output location for this ramp voltage is on the Modulus 9 board, DAC1 out, pin 21. The ramp output voltage from this formula node is connected to the array output voltages for the Modulus 9, Modulus 10, and Modulus 11 boards and written to the same data output file, OUTPUT.TXT, in the fourth column, for analysis and printing. The ramp voltage input is also displayed on the front panel as "Voltage In 1". For a more detailed discussion of this development with accompanying figures refer to Appendix A. This design allows each interferometer transfer function to be obtained in Chapter III through LabVIEW.

4. Automation of Data Collection

The next step in the design involves the limitations of data acquisition with the HP1631D Logic Analyzer. The limitations are listed below:

1. Can only collect up to 1024 data points. If there are more than 1024 data points, the first 1024 points can be collected, then downloaded to the HP disk, then the process must be restarted with data point 1025...etc
2. The HP diskette and text format must be changed through a complex process to obtain an Ascii text file for analysis and printing.

The complexity of handling the data analysis with the outdated HP system is the reason for wanting data collection and analysis within LabVIEW. This problem is addressed in CRAIG8.VI.

In CRAIG8.VI, a sequence structure for data acquisition is nested within the array output voltages loop. Sequence "0" contains a wait 750 ms (3/4 second) timer. Sequence "1" utilizes the sample channels VI to sample analog input channels on the Modulus 9 board, ACH0-ACH8, pins 3,5,7,9,11,13,15,17, and 4. The word output is taken from the Analog-to-Digital Converter circuit board in to the pins listed above. The least significant bit is connected to pin 3, the most significant bit to pin 17, and the parity bit to pin 4. With the write to spreadsheet file VI the voltage data is written to the file, INPUT.TXT. It is then necessary to convert this voltage data to binary format ie., "1" 's and "0" 's. This is accomplished by running the voltages through a comparator bank simulated within LabVIEW. The comparators are located outside of the sequence structure but still within the array output voltages loop. One comparator is used for each bit for a total of nine comparators. Each comparator threshold is set at 2.5 volts. If the voltage taken from the Analog-to-Digital Converter bit is greater than or equal to 2.5 volts a binary "1" is output. If the voltage is less than 2.5 volts a binary "0" is output. This binary word data is then written to a spreadsheet file, WORD.TXT, using the write to spreadsheet file VI, for analysis and printing. For a more detailed discussion of this development with the corresponding figures refer to Appendix A.

III. OPTICAL SYSTEM COMPONENTS

A. OVERVIEW

Each component in the 8-bit design is illustrated in Figure 2 with the corresponding symbols described in Figure 3. Except for the Mach-Zhender interferometers, which are designed by the Naval Research Lab (NRL), there are several choices available for each component. This section of the thesis examines the advantages and disadvantages of each component.

B. LASER TRANSMITTERS

Three laser transmitters are examined and compared. It is desirable to have a Laser Transmitter with as much power as is affordable to supply the system with sufficient power. A high amplitude pulse is desirable at the output of the amplifiers to enable the circuit boards to recognize the pulse. The comparators on the circuit boards are designed by LT Rick Walley, and LT Hiromichi Yamokoshi to work with an amplitude of 2.5 V. The design requires a sampling rate of 5 Mb/s. Considering the bit resolution and sampling rate, the pulsewidth requirement is 20 ns. The Mach-Zhender interferometers are designed by NRL to operate at 1300 nm.[Ref. 1] Some of the desired characteristics are conflicting ie., a high amplitude and a narrow pulsewidth. This creates trade-offs within the scope of the system design.

1. BCP 400

Broadband Communications Products, Inc. makes the BCP 400 Laser Transmitter. The Optical Electronics Laboratory in Bullard Hall has three of these transmitters. The Model 400 is a high speed optical signal source with a maximum bit rate of 1.3 Gb/s. The 400 is capable of accepting both analog and digital inputs out to 1 GHz. The 400 produces a fiber-coupled optical output and is used in the digital mode in this thesis research. In the digital mode the 400 accepts an input pulse pattern from DC to sub-nanosecond pulses in continuous or burst mode. The pulsewidth of the optical output

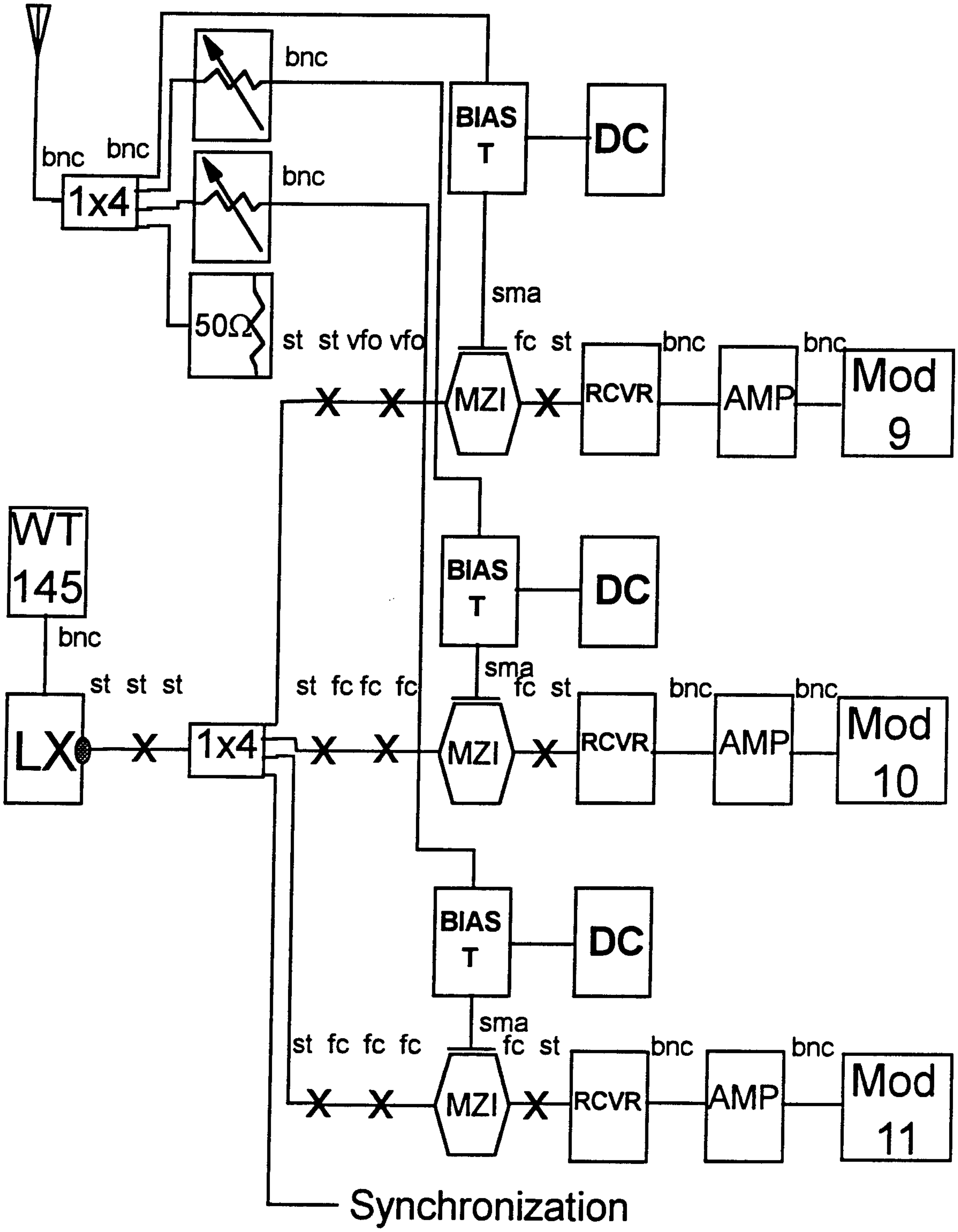


Figure 2. 8-Bit Optical System Diagram

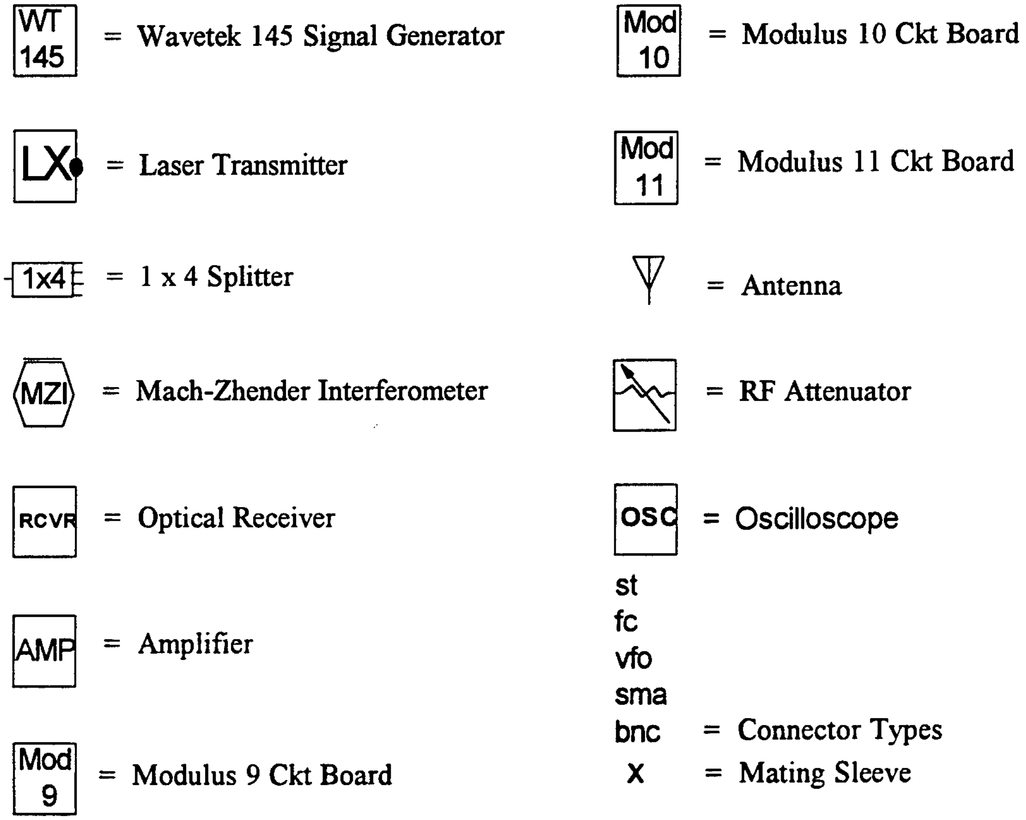


Figure 3. Symbol Diagram Dictionary

can be adjusted on the front panel with the digital input logic threshold potentiometer. On the rear panel of the Model 400 one can adjust the laser bias point which allows limited control of waveform characteristics and extinction ratio. The Model 400 parameters of interest for this research are listed in Table 1. [Ref. 9]

Parameter	**Characteristic**
Bit Rate	1.3 Gb/s
Pulse Pattern	No Constraint, any combination
Digital-Output Optical	
Pulse Rise/Fall Times	0.5 nsec (max.)
Minimum Pulse Width	0.75 ns
Extinction Ratio	10:1 (min.)
Peak Coupled Power	0.75 mw into (8/125) fiber
Wavelength	1300 nm
Spectral Width	4 nm

Table 1. BCP 400 Specifications

The setup for testing and evaluation of the BCP 400 is exhibited in Figure 4. The Model 400 is tested for minimum pulsewidth and maximum pulse amplitude. To obtain minimum pulsewidth the digital input of the Model 400 is driven with a Wavetek 145 Signal Generator with the triangle function selected. By alternately adjusting the threshold potentiometer on the front panel of the BCP 400 and the DC offset on the Wavetek 145, the pulsewidth can be varied. This is shown in Figure 5. A minimum pulsewidth of 4 ns can be obtained in the lab as shown in Figure 6. The potentiometer and DC Offset are not fine enough to go below 4 ns. However, for the purpose of the system design which

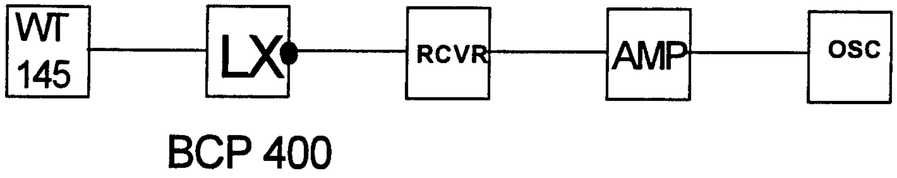


Figure 4. Setup For Testing BCP 400 Laser Transmitter

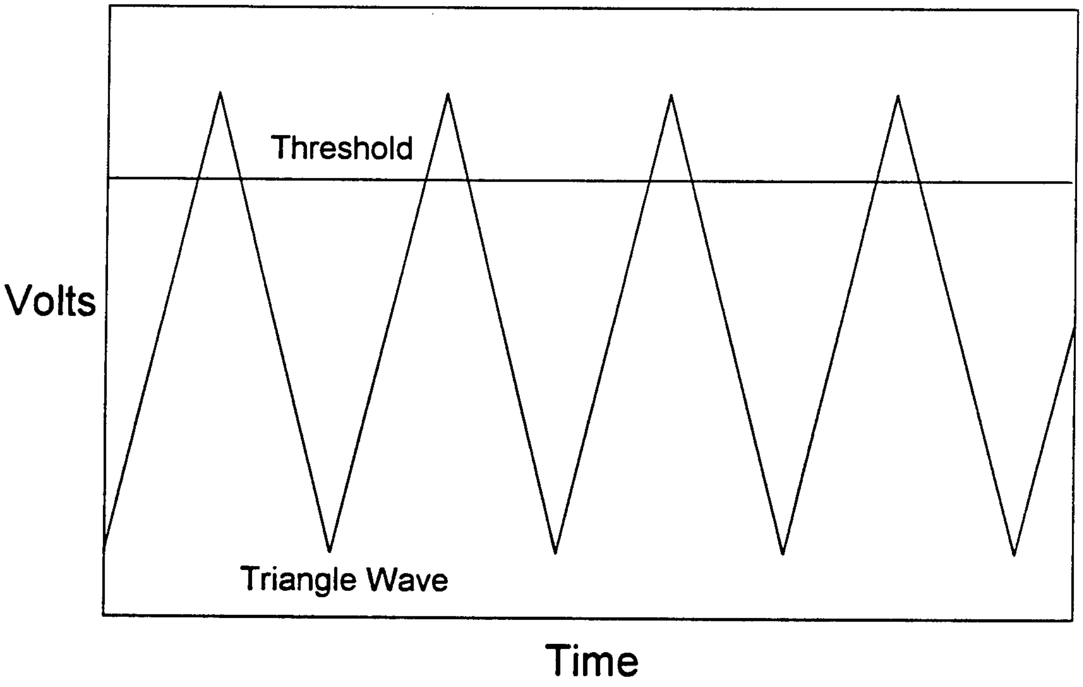


Figure 5. Method to Obtain Minimum Pulsewidth

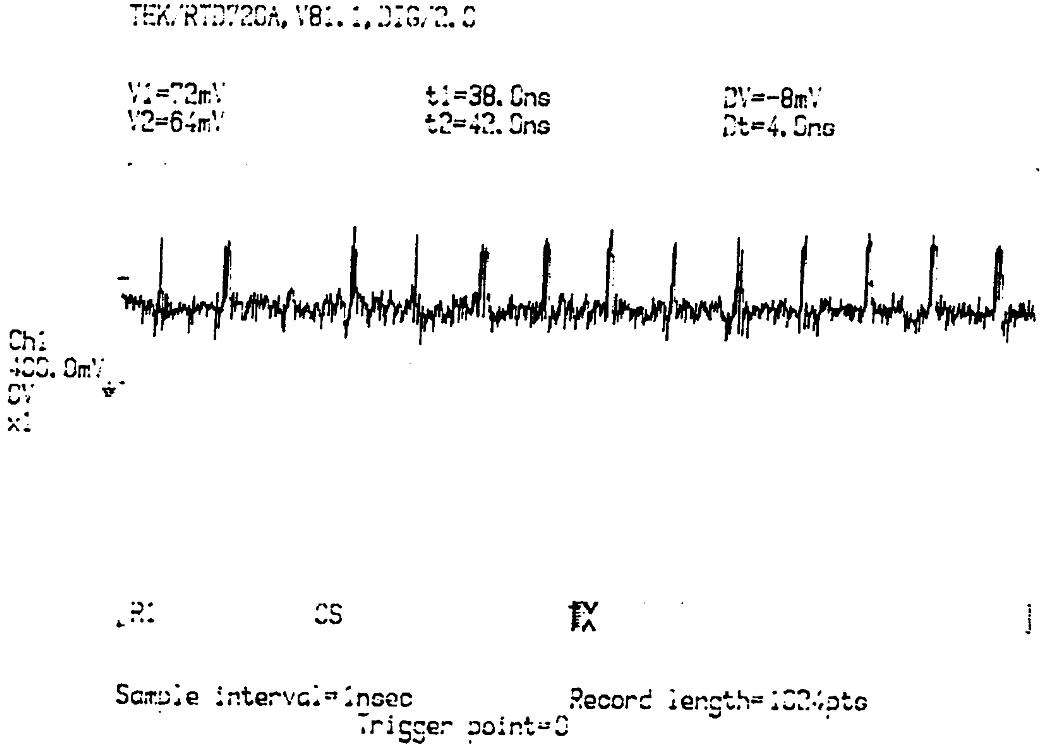


Figure 6. BCP 400 Minimum Pulsewidth And Maximum Amplitude

requires a 20 ns pulsewidth, the BCP 400 is more than adequate. In Figure 6, the maximum pulse amplitude is shown as 72 mV.

Advantages: The Optical Electronics Laboratory has three model 400 lasers in its inventory. The specified system data rates and pulsewidths are obtainable with the BCP 400.

Disadvantages: The output power of the BCP 400 is low compared to other laser transmitters on the market.

2. BCP 410A

Broadband Communications Products, Inc. also makes the BCP 410A Laser Transmitter. Although the Optical Electronics Laboratory in Bullard Hall has three of the BCP400 models, NPS doesn't have any of the BCP410A's. The Optical Electronics Laboratory is able to borrow one BCP 410A Laser Transmitter from Broadband Communications for consideration in this research.

The Model 410A is similar in many respects to the Model 400. The Model 410A is a high speed optical signal source with a maximum bit rate of 2.0 Gb/s. The 410A is capable of accepting both analog and digital inputs out to 1.5 GHz. The 410A produces a fiber-coupled optical output and is used in the digital mode in this thesis research. Like the Model 400, in the digital mode the 410A accepts an input pulse pattern from DC to sub-nanosecond pulses in continuous or burst mode. The pulsewidth of the optical output can be adjusted on the front panel with the digital input logic threshold potentiometer. On the rear panel of the Model 410A one can adjust the laser bias point which allows limited control of waveform characteristics and extinction ratio. The Model 410A parameters of interest for this research are listed in Table 2. [Ref. 10]

The setup for testing and evaluation of the BCP 410A is the same as used for the BCP 400 as shown in Figure 7. Like the Model 400 the Model 410A is tested for minimum pulsewidth and maximum pulse amplitude as shown in Figure 8. The same method for obtaining minimum pulsewidth is used for the Model 410A as with the Model 400. The 410A is driven with a Wavetek 145 Signal Generator with the triangle function

Parameter	**Characteristic**
Bit Rate	2.0 Gb/s
Pulse Pattern	No Constraint, any combination
Digital-Output Optical	
Pulse Rise/Fall Times	0.4 nsec (max.)
Minimum Pulse Width	0.5 ns
Extinction Ratio	10:1 (min.)
Peak Coupled Power	1.0 mw into (9/125) fiber
Wavelength	1300 nm
Spectral Width	0.7 nm

Table 2. BCP 410A Transmitter Specifications

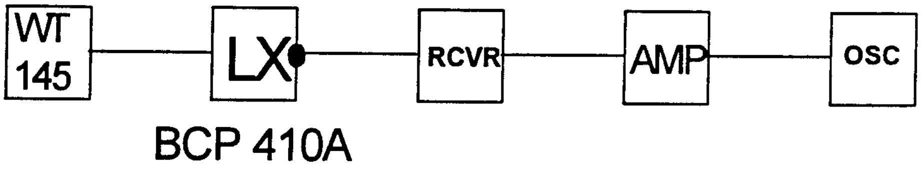
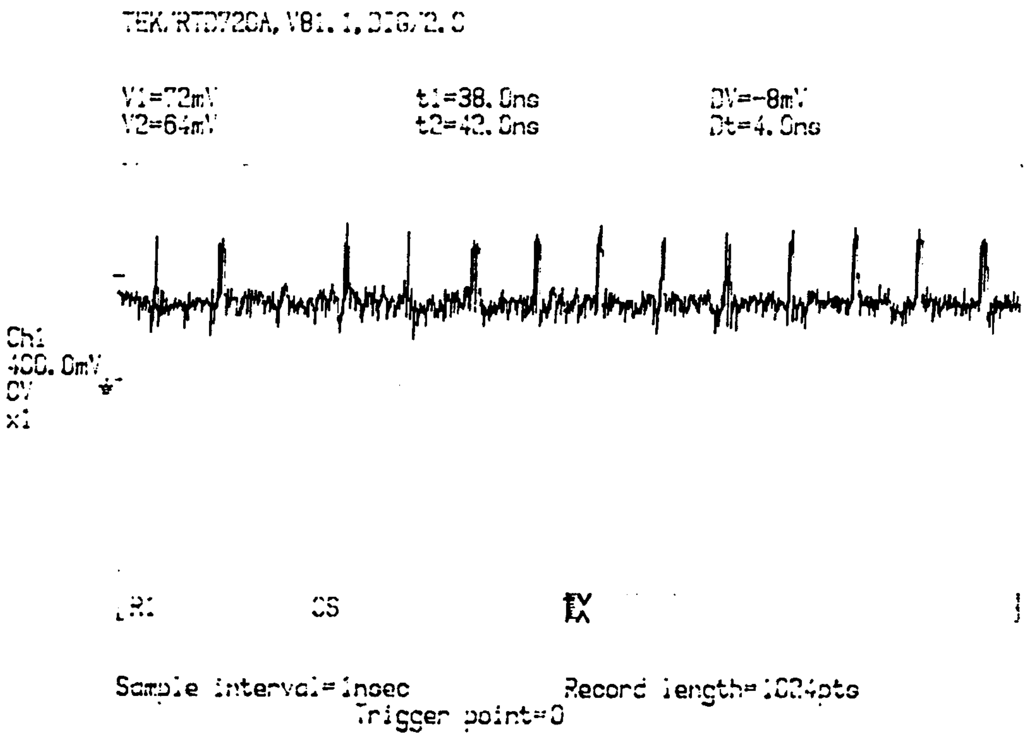


Figure 7. Setup For Testing BCP 410A



```
TEK/RTD720A,V81.1,DIG/2.0

V1=72mV              t1=38.0ns             DV=-8mV
V2=64mV              t2=42.0ns             Dt=4.0ns

Sample interval=1nsec             Record length=1024pts
                    Trigger point=0
```

Figure 8. BCP 410A Minimum Pulsewidth And Maximum Amplitude

selected. By alternately adjusting the threshold potentiometer on the front panel of the BCP 410A and the DC offset on the Wavetek 145, the pulsewidth can be varied, see Figure 4. Using this method a minimum pulsewidth (Figure 8) of 4 ns is obtainable in the lab. The potentiometer and DC Offset are not fine enough to go below 4 ns. However, for the purpose of the system design which requires a 20 ns pulsewidth, the 4 ns pulsewidth is more than adequate. In Figure 8, the maximum pulse amplitude obtainable in the lab is 72 mV.

Advantages: None noted.

Disadvantages: The Optical Electronics Laboratory doesn't have any BCP 410A laser transmitters in its inventory. The cost to purchase one BCP 410A is approximately $7,000. There are no advantages in pulsewidth, data rate, or output power that make the BCP 410A desirable over the BCP 400 for this thesis research.

3. Mode Interlock

Lightwave Electronics makes the Series 131-1047-100 and the Series 131-1047-200 mode interlock laser transmitters. The only difference between the specifications for the two models is in power. The Series 131-1047-100 has an average power of 100 mW whereas the Series 131-1047-200 has an average power of 200 mW. NPS doesn't have either of these models. The cost to purchase either of these models, $35K to $50K, exceeds the current budget. The Series 131 model is interesting for consideration in future research primarily due to the large increase in output power above the BCP 400 Laser Transmitter that is currently being used.

The Series 131 laser produces picosecond pulses with wavelengths near 1000 nm with a standard repetition rate of 100 MHz. If this is not satisfactory, the pulsewidths and repetition rates can be built to the user's specification. The pulses have a low level of noise and exhibit low timing jitter so that it can be used in precision pulse applications. The Series 131 can be built with a standard repetition rate in the range of 75 to 250 MHz. The repetition rate can not be adjusted by the user because it is fixed at the time of construction. The items of interest for future research consideration are detailed in Table 3.[Ref. 11]

Parameter	Specification
Wavelength	1047 nm
Pulse Width	< 10 ps
Repetition Rate	100 MHz (Standard)
Average Power	> 100 mW
Jitter (1 Hz to 10 kHz)	< 1 ps rms
Amplitude Noise (1 Hz to 1 MHz)	< 1% rms
Polarization, linear	> 100/1, horizontal

Table 3. Series 131 Mode Interlock Transmitter Specifications

Advantages: The Series 131 laser has a significant increase in power over that of the BCP 400 currently in use. It also has identifiable picosecond jitter.

Disadvantages: The Series 131 is beyond the current budget.

C. NRL MACH-ZHENDER INTERFEROMETERS

1. Modulator Performance

The three Mach-Zhender interferometers used in this research are designed at the NRL and are on loan from the National Security Agency (NSA). The maximum voltage that can be applied to these devices is $v_{max} = 31.875V$. The V_π is 2.25 volts for the Modulus 9 interferometer, the minimum modulus. The total number of folds available from each device is 14.17. Refer to Chapter IV for the calculations of these values. Don Lafaw, an engineer at University of Maryland, College Park, tested them for insertion loss, phase angle ablation, and phase angle thermal stability. The insertion loss for the three interferometers at zero degree phase is illustrated in Table 4. The Phase Angle (deg) Ablation aimed at 89.3 degrees is documented in Table 5. The phase angle thermal stability of each device is documented in Table 6.[Ref. 12]

Device	Initial (dB)	Final (dB)
M3d	11.9	12.8
M8b	7.7	7.8
M9c	9.4	10.6

Table 4. Interferometer Insertion Loss

Device	Original	At end of ablation	1-2 days after ablation	Final
M3d	149.9	89.4	89.3	89.4
M8b	131.7	89.7	89.6	90.1
M9c	145.1	89.5	87.3	88

Table 5. Interferometer Phase Angle Ablation

2. Characteristic Waveforms

Each interferometer has a characteristic waveform with the shape of a $(\cos)^2$ function. The waveforms for each interferometer are obtained in the lab by providing a ramp voltage input to the interferometer. The voltage ramps between -32 V and + 32 V. The ramp voltage is supplied through a VI created in LabVIEW, MZIRAMP.VI. This program also collects the output voltage of the interferometer and writes this data to a text file for further analysis and printing. The interferometer output voltage text file is

Device	Temp T (°C)	Before Ablation			After Ablation		
		Angle (deg)	Change (deg)	(deg/°C)	Angle (deg)	Change (deg)	(deg/°C)
M3d	20 - 22	149.8			89.4		
	40 - 41	149.4	-0.4	-0.019	88.5	-0.9	-0.049
	-21 - -24	151.6	1.8	0.044	92.1	2.7	0.059
M8b	20 - 22	131.8			91.5		
	40-41	131.5	-0.3	-0.016	91.1	-0.4	-0.022
	-21- -24	135.9	4.1	0.094	95.8	4.3	0.093
M9c	20 - 22	145.1			87.1		
	40 - 41	145.8	0.7	0.036	85.7	-1.4	-0.0740.
	-21- -24	145.5	0.4	0.009	89.8	2.7	0.059

Table 6. Interferometer Phase Angle Thermal Stability

named, MACHZOUT.TXT. For a more detailed discussion of MZIRAMP.VI refer to Appendix A.

The ramp voltage input to the interferometers is displayed in Figure 9. The characteristic waveform for each of the three interferometers is illustrated in Figure 10, Figure 11, and Figure 12.

D. OPTICAL RECEIVERS

Four optical receivers are examined and compared. It is desirable to have a low-noise optical receiver operating at a wavelength of 1320 nm with a wide bandwidth and a high-gain that will enable the low-noise detection of a signal at the output of the interferometers. The optical receiver must also permit a data rate of 5 Mb/s and handle a

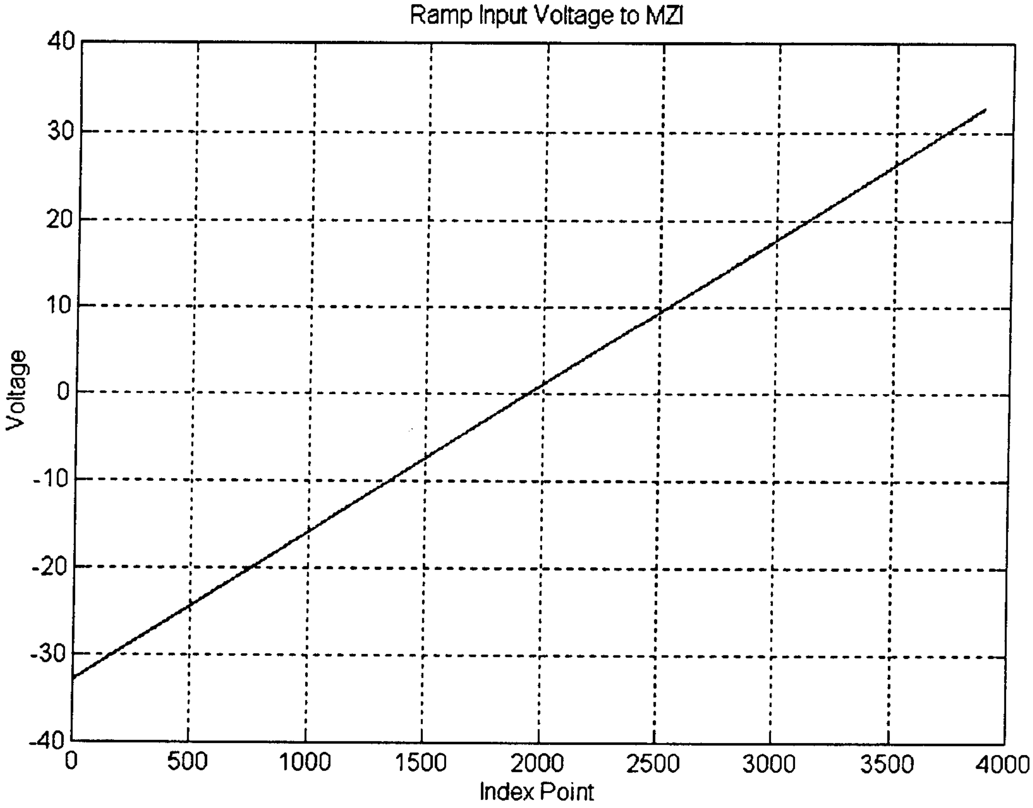


Figure 9. Ramp Input Voltage To Interferometers

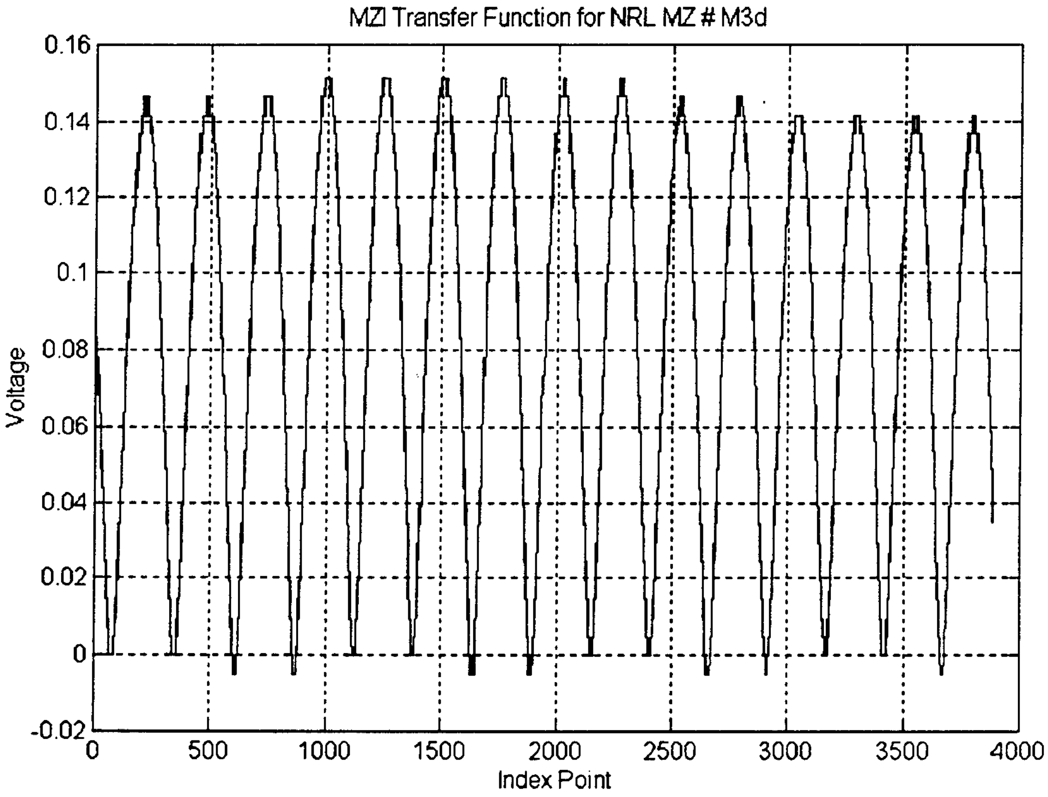


Figure 10. Characteristic Waveform of NSA Interferometer M3b

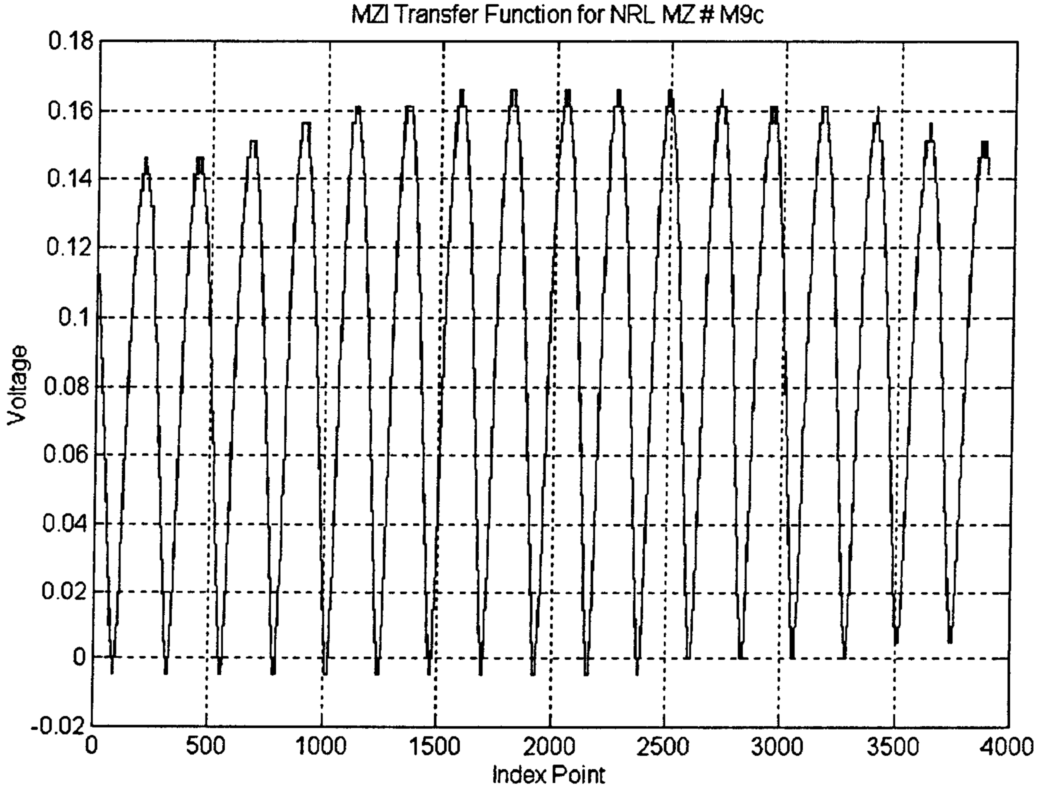


Figure 11. Characteristic Waveform of NSA Interferometer M9c

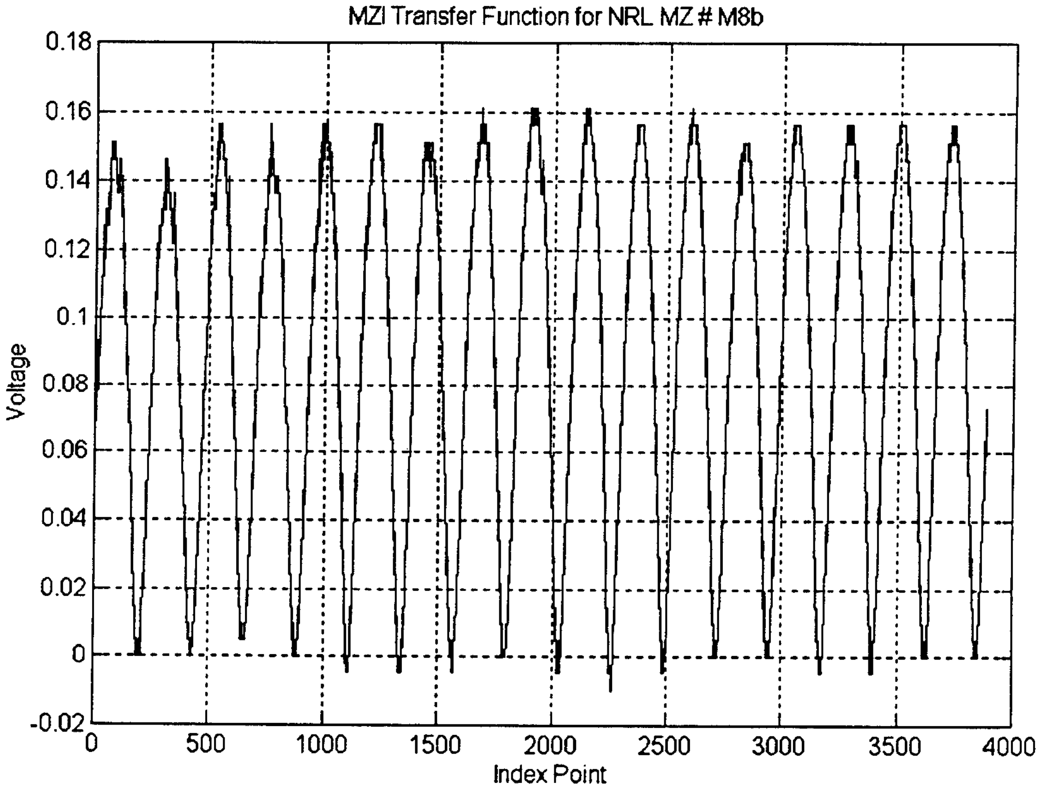


Figure 12. Characteristic Waveform of NSA Interferometer M8b

pulsewidth as small as 1 ns. A variable gain is also desirable to adjust for unequal outputs at the output of the interferometers. Some of the desired characteristics are conflicting ie., a wide bandwidth and high-gain. This creates trade-offs within the scope of the system design.

1. New Focus 1611

The Optical Electronics Laboratory has three New Focus Model 1611 photoreceivers in its inventory. The 1611 is a low-noise photoreceiver that consists of an InGaAs PIN photodiode followed by a low-noise amplifier. The Model 1611 parameters of interest for this research are listed in Table 7.[Ref. 13]

Parameter	**Characteristic**
Coupling	DC or AC
Bandwidth (3dB)	DC-1 GHz (typ. DC) 25kHz-1GHz (typ. AC)
Photodiode Material	InGaAs PIN
Power Requirements	$\pm 15V$ DC; 300 mA
Risetime	0.5 ns (typ.)
Current Gain	250 V/A (typ.)
Input Noise Current	$11 pA/\sqrt{Hz}$ @ freq.> 1 MHz
Output Current	40 mA (max into 50 Ω)
Maximum Input Power	5 mW (max @ 1.3 μm)
Dynamic Range	> 60 dB (typ.)

Table 7. New Focus 1611 Specifications

Advantages: The receiver's 1 GHz BW permits pulsewidths as low as 1 ns and allows 5 Mb/s data rate. The Optical Electronics Laboratory has three Model 1611 photoreceivers in inventory.

Disadvantages: Gain is lower than with the BCP 310A receiver. This model does not have a variable gain adjustment.

2. New Focus 1811

The Optical Electronics Laboratory has one New Focus Model 1811 photoreceiver in its inventory. The 1811 is a low-noise photoreceiver that consists of an InGaAs PIN photodiode followed by a low-noise amplifier. The Model 1811 parameters of interest for this research are listed in Table 8.[Ref. 14]

Parameter	**Characteristic**
Coupling	DC or AC
Bandwidth (3dB)	DC-125 MHz (typ. DC) 25kHz-125 MHz (typ. AC)
Wavelength Range	800-1800 nm
Photodiode Material	InGaAs PIN
Power Requirements	$\pm 15 V$ DC; 250 mA
Risetime	3 ns (typ.)
Current Gain	40 V/mA (typ.)
Input Noise Current	$2 pA/\sqrt{Hz}$ @ 10 MHz (typ.)
Output Current	40 mA (max into 50 Ω)
Maximum Input Power	5 mW (max @ 1.3 μm)

Table 8. New Focus 1811 Specifications

Advantages: Gain is higher than with the New Focus 1611.

Disadvantages: Receiver cannot handle 1 ns pulsewidth due to 125 MHz BW. Gain is lower than with the BCP 310A and is not variable.

3. BCP 300

The Broadband Communications Products (BCP) Model 300 is an optical receiver that is designed for detection of high speed optical signals. The receiver utilizes DC coupled avalanche detectors and handles wavelengths in the range 500-1550 nm. The gain of the detector is adjustable with a potentiometer knob on the front panel of the device. The BCP 300 includes a 26 dB AC-coupled amplifier. The 26 dB amplifier can be used at the output of the detector or independently as a general purpose amplifier. The BCP 300 parameters of interest for this research are listed in Table 9.[Ref. 15]

Parameter	**Characteristic**
Coupling	DC
Bandwidth (3dB)	2KHz-700 MHz
Wavelength Range	500-1550 nm
Photodiode Material	Germanium APD
Power Requirements	120/240 VAC
Sensitivity @ max. gain (50 Ω termination)	400 V/W (min, 1300 nm)
Sensitivity @ min. gain (50 Ω termination)	40 V/W (max, 1300 nm)
Input Equivalent Noise Current	400 nA RMS (typ., full BW)
Maximum Output	0.5 V p-p (min)

Table 9. BCP 300 Optical Receiver Specifications

Advantages: Receiver has high sensitivity and gain. Receiver has a variable gain adjustment which is a desirable feature.

Disadvantages: Gain and sensitivity are lower than with the BCP 310A. Receiver maximum output is only 0.5 V p-p.

4. BCP 310A

The Broadband Communications Products (BCP) Model 310A is a wideband, high speed optical-to-electrical (O/E) conversion instrument. The BCP 310A parameters of interest for this research are listed in Table 10.[Ref. 16] The BCP 310A consists of three independent blocks:

1. High gain wide bandwidth O/E converter.
2. Linear amplifier.
3. ECL limiting amplifier.

The O/E converter consists of a DC-coupled detector and amplifier with a very high gain and wide bandwidth. Optical signals in the range 100 nW - 100 μW can be

Parameter	**Characteristic**
Coupling	DC
Bandwidth (3dB)	0-1500 MHz
Wavelength Range	1100-1600 nm
Photodiode Material	Germanium APD
Power Requirements	120/240 VAC
Conversion Gain	10,000 V/W (1300 nm)
Minimum Discernable Signal (MDS)	20 nW
Maximum Output	0.5 V p-p (min)
Amplifier Gain	20 dB

Table 10. BCP 310A Optical Receiver Specifications

detected. The output signal amplitude is adjustable with a potentiometer knob located on the front panel of the device. The linear amplifier is AC coupled and can be used at the output of the detector or independently as a stand alone amplifier. The ECL limiting amplifier allows the Model 310A to be used for optical source bit error rate (BER) testing.[Ref. 16]

Advantages: Gain and bandwidth are higher than with the other receivers examined. This is the most sensitive device of the four examined. The receiver includes a variable gain feature that is desirable within the system design.

Disadvantages: Amplifier section only has a 20 dB gain compared to a 26 dB gain with the BCP 300 receiver/amp. The maximum output of the receiver is 0.5 V p-p.

E. AMPLIFIERS

The system needs an amplifier with high variable gain to adjust for uneven outputs from the interferometers, wide bandwidth performance, and linear operation within the bandwidth of interest (0-1GHz). Four Amplifiers are examined.

1. BCP 300

The BCP 300 optical receiver is detailed in the preceding section. This device consists of a detector with an amplifier that can be used at the output of the detector or independently. The characteristics of the BCP 300 amplifier are listed in Table 11.[Ref. 15]

Parameter	**Characteristics**
Gain	26 dB (typ., non-inverting)
Bandwidth (-3dB)	2 KHz - 700 MHz
Maximum Output	0.5 V peak to peak

Table 11. BCP 300 Amplifier Specifications

Advantages: This amplifier's 26 dB gain is higher than the 20 dB gain with the BCP 310A and is variable.

Disadvantages: The bandwidth is smaller than with the BCP 310A amplifier. Maximum output from the amplifier is only 0.5 V p-p.

2. BCP 310A

The BCP 310A optical receiver is detailed in the preceding section. This device consists of a detector with a built in amplifier that can be used at the output of the detector or independently as a stand alone amplifier. The characteristics of the BCP 310A amplifier are listed in Table 12.[Ref. 16]

Parameter	**Characteristics**
Gain	20 dB (typ., non-inverting)
Bandwidth (-3dB)	0.1 - 1500 MHz
Maximum Output	0.5 V peak to peak

Table 12. BCP 310A Amplifier Specifications

Advantages: Amplifier gain is variable.

Disadvantages: Bandwidth is larger than with the BCP 300 amplifier. Maximum output from the amplifier is only 0.5 V p-p.

3. HP 8447A

The HP 8447A is a wideband RF amplifier. The characteristics of the HP 8447A amplifier are documented in Table 13.[Ref. 17]

Advantages: Maximum amplifier output voltage is 10 V.

Disadvantages: Amplifier bandwidth is only 0.1 - 400 MHz and its gain of 20 dB is not adjustable.

Parameter	Characteristics
Gain	20 dB (typ., non-inverting)
Bandwidth (-3dB)	0.1 - 400 MHz
Maximum Output	10 V DC Maximum

Table 13. HP 8447A Amplifier Specifications

4. HP 8347A

The HP 8347A is a broadband instrumentation amplifier with a variable gain feature. The characteristics of the HP 8347A are listed in Table 14.[Ref. 18]

Parameter	Characteristics
Gain	25 dB (typ., non-inverting)
Bandwidth (-3dB)	100 KHz - 3.0 GHz
Maximum Output	> 10 V DC Maximum

Table 14. HP 8347A Specifications

Advantages: This amplifier has a high variable gain. The BW is higher than with the other models examined. Maximum amplifier output voltage is greater than 10 V.

Disadvantages: The amplifier's 25 dB gain is one dB lower than with the 26 dB gain of the BCP 300 amplifier discussed above.

F. SINGLE MODE FIBER AND CONNECTORS

Single Mode fiber is used throughout the optical path in the 8-bit design with the exception of the three polarization maintaining fiber leads at the inputs to the Mach-Zhender interferometers. This section of the research looks at some of the possible design limitations with single mode fiber.

The types of nonlinear scattering of light when only one wavelength is present are Brillouin and Raman Scattering. With low power laser transmitters, the scattering is negligible. However, with high power laser transmitters, significant power loss can occur from scattering.

1. Brillouin Scattering

Brillouin Scattering arises from the modulation of the light traveling through the fiber by the thermal energy of the fiber. The optical power level of significant Brillouin Scattering is given by

$$P_b = a^2 \lambda^2 \alpha \Delta v \tag{22}$$

where

P_b is the power level (W) required for Brillouin Scattering to start,

a is the fiber radius (μm),

λ is the source wavelength (μm),

α is fiber loss in dB/km,

and Δv is the source linewidth (GHz).

If the power level of the light traveling through the fiber is above this threshold there will be losses due to Brillouin Scattering.[Ref. 19]

For the 8-bit system there are two types of single mode fiber in use. The first type of fiber is the 50 μm diameter fiber used before and after the interferometers. The second type of fiber is the 8 μm diameter polarization maintaining fiber leads at the inputs to the interferometers.

For the 50 μm diameter fiber, a=25μm, λ=1.3μm, α=0.1 dB/Km (Assume), and

$$\Delta v = \frac{c}{\lambda^2}\Delta\lambda = \frac{3\times10^8}{\left(1300\times10^{-9}\right)^2}(4\times10^{-9}) = 710\ GHz$$

therefore,

$$P_b = (17.6\times10^{-3})(25)^2(1.3)^2(0.1)(710) = 1.3\ KW\,. \tag{23}$$

For the 8 μm diameter polarization maintaining fiber, a=4μm, λ=1.3μm,α=0.16 dB/Km (Assume), and Δv=710GHz therefore,

$$P_b = (17.6 \times 10^{-3})(4)^2(1.3)^2(0.16)(710) = 54.1\ W. \tag{24}$$

From these results it is evident that the 8-bit system with a power level of 0.75 mW at the BCP 400 Laser Transmitter will have negligible losses from Brillouin Scattering.

2. Raman Scattering

Raman Scattering is produced when there is a nonlinear interaction between the light traveling through the fiber and the fiber producing a high-frequency phonon. Significant Raman Scattering occurs when the power of the source rises above the threshold determined by

$$P_R = (23.6 \times 10^{-2})a^2\lambda\alpha \tag{25}$$

where P_R is in Watts, and a, λ, and α are the same quantities defined above in the Brillouin Scattering section.[Ref. 19]

Again, for the 8-bit system there are two types of single mode fiber in use. The first type of fiber is the 50 μm diameter fiber used before and after the interferometers. The second type of fiber is the 8 μm diameter polarization maintaining fiber leads at the inputs to the interferometers.

For the 50 μm diameter fiber,

$$P_R = (23.6 \times 10^{-2})(25)^2(1.3)(0.1) = 19.2\ W. \tag{26}$$

For the 8 μm diameter polarization maintaining fiber,

$$P_R = (23.6 \times 10^{-2})(4)^2(1.3)(0.16) = 785.4\ mW. \tag{27}$$

From these results it is evident that the 8-bit system with a power level of 0.75 mW at the BCP 400 Laser Transmitter will have negligible losses from Raman Scattering.

It is also evident that the limiting factor for scattering within the 8-bit system is Raman Scattering with a threshold of 785.4 mW.

3. Polarization Maintaining Fiber

Mach-Zhender interferometers are phase sensitive devices. Because of this, they are constructed with input leads that are polarization maintaining. The three Mach-Zhender interferometers used in the 8-bit design have single-mode polarization maintaining fiber leads at their inputs. The BCP 400 Laser Transmitter is connected to the input of each interferometer through a single-mode 1X4 splitter and single-mode fiber, both of which are non-polarization maintaining. There is no way to control or maintain the polarization of the light coming out of the BCP 400 Laser Transmitter since the laser produces polarized light but the angle of adjustment is not known by the manufacturer. There is no way to maintain the polarization of the light traveling through the single-mode fiber since it doesn't retain the polarization of the input source .[Ref. 20] However, the polarization of the light can be adjusted between the polarization maintaining fiber input leads and the single-mode fiber to allow maximum power output if the connection at this mating is rotatable. This requirement forced the purchase of Polarization Maintaining Connectors discussed next.

4. Polarization Maintaining Connectors

It is necessary to be able to rotate the connection between the interferometer polarization maintaining fiber input leads and the non-polarization maintaining single-mode fiber. Polarization Maintaining Connectors allow this to be done.

Fiber Instrument Sales (FIS) makes a FC to ST mating sleeve that can be adjusted for maximum power output. The FC side of the connection is not keyed as in a normal FC type connector. This permits this side to be rotated. To adjust the polarization to achieve maximum power output, one loosens the FC side of the connection and rotates the connection while simultaneously observing the Oscilloscope with a display of the output waveform. When the maximum amplitude of the waveform is obtained, the FC connection is screwed tight locking it into position and maintaining the maximum output power setting. Each interferometer connection is made with this type of mating sleeve and is adjusted for maximum power output.

IV. 8-BIT SNS ADC SYSTEM FINAL CONFIGURATION

A. COMPONENTS

Each of the components under consideration for the 8-bit design are discussed in detail in Chapter III with each of their advantages and disadvantages. The 8-bit system diagram is displayed again in Figure 13. The system diagram dictionary is displayed in Figure 14. The components chosen for each part of the system and the reasons for their selection are discussed below.

The BCP 400 Laser Transmitter is used as the source because the Optical Electronics Laboratory has three of the Model 400 units in inventory. If the budget allowed the purchase of another source for this design it would be the Series 131 Mode Interlock Laser produced by Lightwave Electronics. The Series 131 is a better choice for the source than the BCP 400 because of greatly increased power, and picosecond jitter rates.

From the BCP 400 the light passes through a 1X4 splitter made by Fiber Instrument Sales. It is used in this design because it allows the even splitting of single-mode light into four outputs. The lightwave then travels through three channels consisting of single-mode fiber into each of the three interferometer polarization maintaining leads. The mating sleeve at this connection point is made by FIS and is polarization adjustable as discussed in Chapter III. From the mating sleeve the lightwave passes through the polarization maintaining fiber into the Mach-Zhender interferometers on loan from the National Security Agency (NSA). The interferometer design specifications and general characteristics are discussed and documented in Chapter III.

After the light passes through the interferometers, it passes through a single-mode fiber into the receivers, one for each channel. The BCP 310A Optical Receiver/Amplifier is the system choice because of its wide bandwidth, high sensitivity, and variable gain wideband amplifier. The lightwave passes through the optical receiver where it is converted to electricity and then passes into the first amplifier stage, the BCP 310A 20 dB

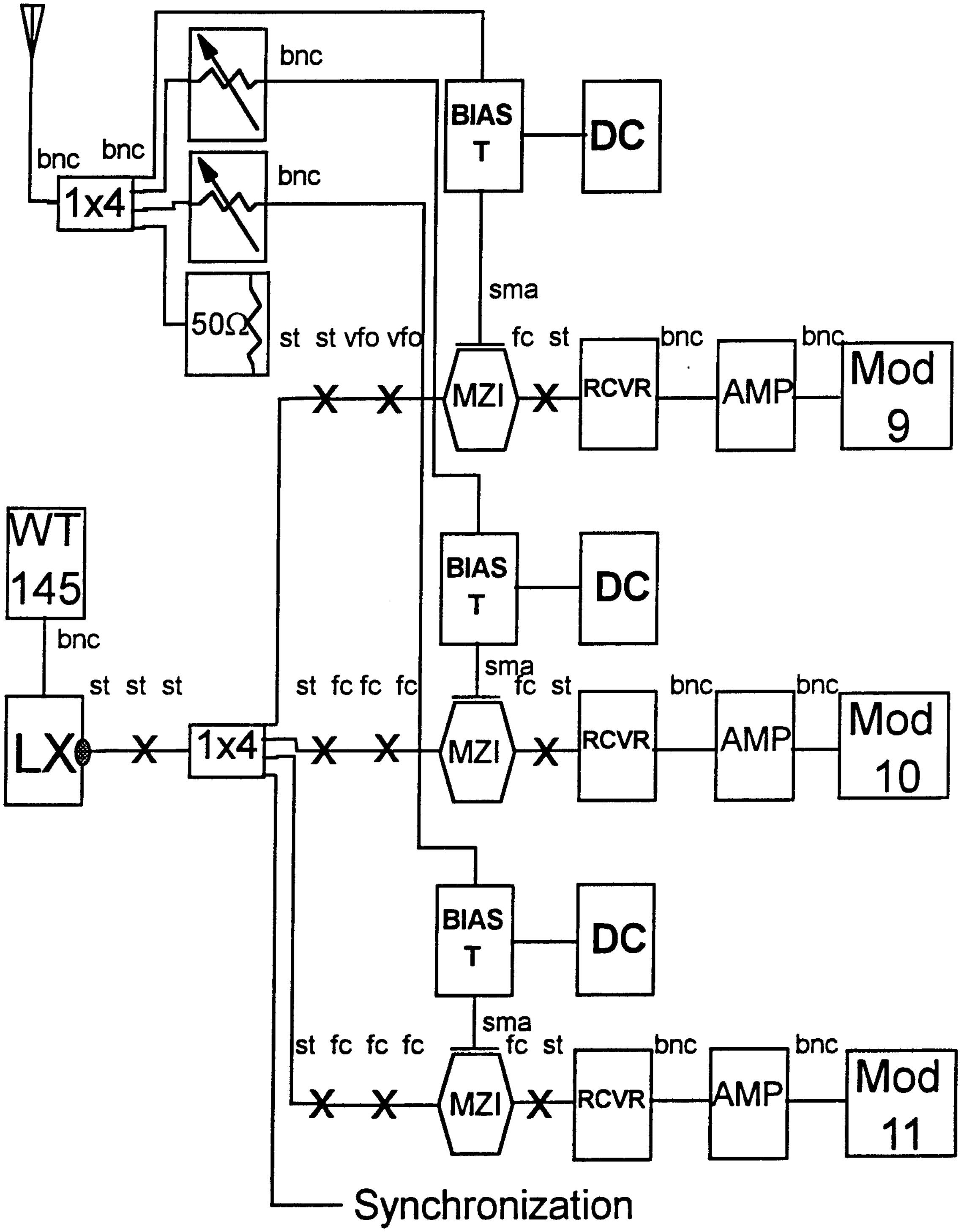


Figure 13. 8-Bit Optical System Diagram

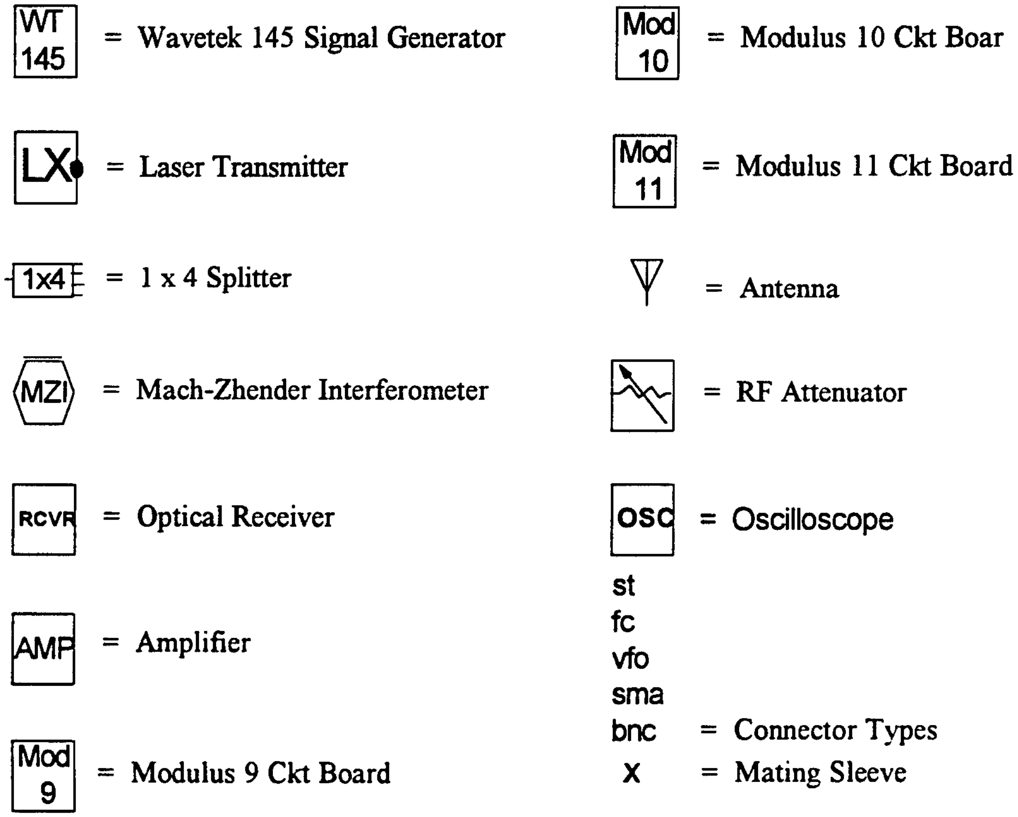


Figure 14. 8-Bit System Diagram Dictionary

amplifier. After the BCP 310A 20 dB amplifier stage the RF energy is sent to the input of the HP8347A amplifier.

The HP8347A instrumentation amplifier is the choice for this system due to its high variable gain and wide bandwidth. After amplification the energy is sent to the digital circuit boards. The digital processor is part of another thesis project and is not discussed here. The second channel across the Mach-Zhender interferometers carries the RF energy. The Modulus 9, Modulus 10, and Modulus 11 interferometers each require a DC bias to tune the interferometer. Tuning of the interferometer is discussed below. The DC bias is provided through a Bias-Tee input where the RF waveform is added to the DC bias. The RF waveform only has to be biased for the Modulus 9 interferometer. For the Modulus 10 and Modulus 11 interferometers the waveform folding period must also be adjusted and this is performed with a RF attenuator in each channel. The RF attenuator is a wideband 20 dB attenuator.

B. LINK BUDGET ANALYSIS

The final configuration of the 8-bit system is detailed above. Here a link budget analysis is performed on the optical portion of the system to measure the insertion losses within the design. The design is divided into three sections as shown in Figure 15. Section #1 consists of the single-mode fiber connection from the laser transmitter through the 1x4 splitter up to the mating sleeve attached to the interferometers. Section #2 starts at the polarization maintaining fiber inputs to the interferometers and ends at the single-mode output lead of the interferometer. Section #3 begins at the mating sleeve at the output of the interferometers and ends at the optical receiver. The insertion loss is measured for each section within each interferometer channel. The measurements are given in Table 15 along with the total insertion loss for each channel. Since the BCP 400 has a power output of 0.75 mW as discussed in Chapter III, the total power at the receiver can be calculated by subtracting the total channel insertion loss from the source power (in dBm) for each channel.

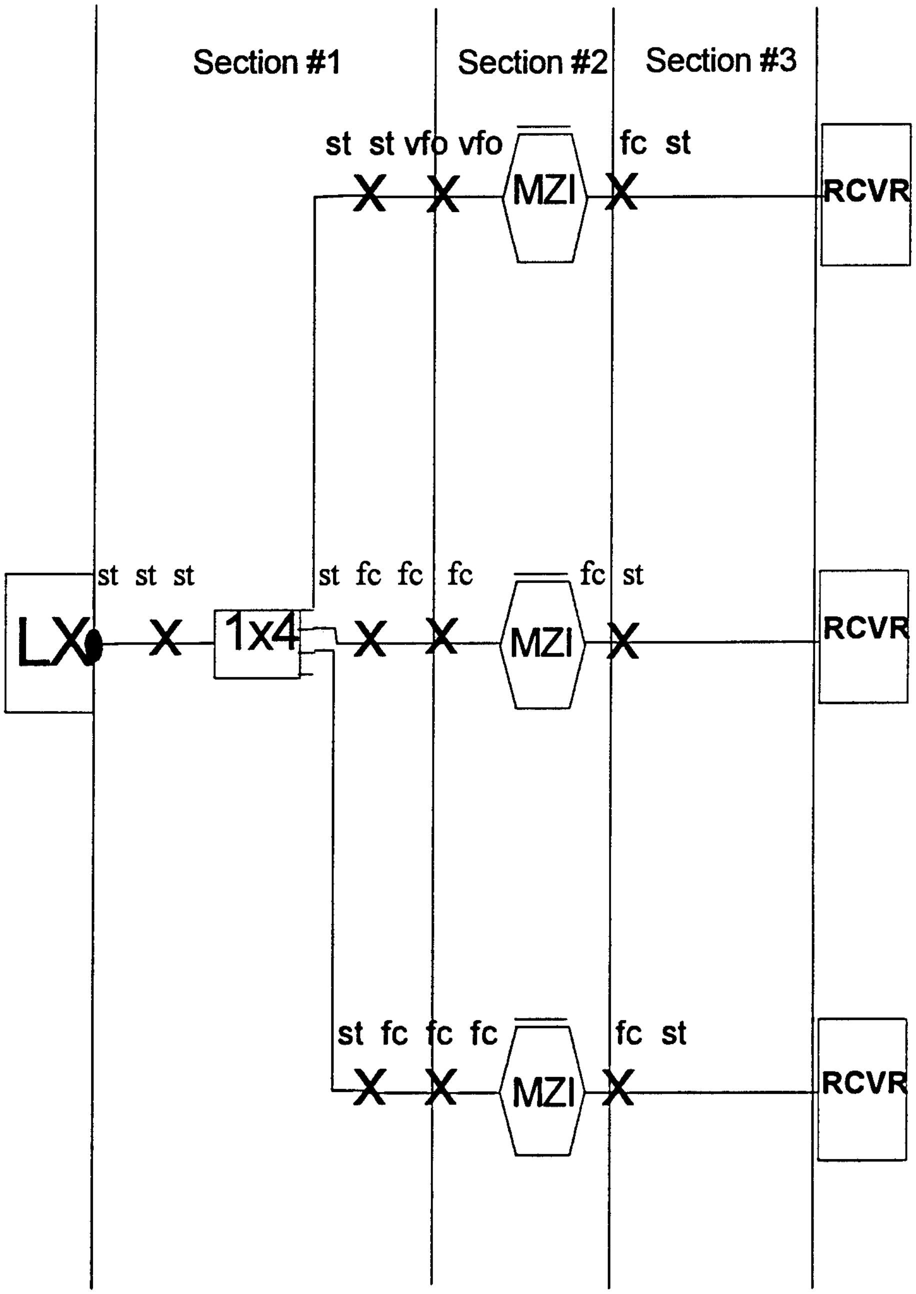


Figure 15. Link Budget Analysis

MZI Channel	Section #1 Loss (dB)	Section #2 Loss (dB)	Section #3 Loss (dB)	Total Loss (dB)	Power At Receiver (dBm)
M3b	-9.1	-12.8	-8.1	-30	-31.25
M9c	-10.9	-7.8	-8.3	-27	-28.25
M8b	-9.8	-10.6	-7.5	-27.9	-29.15

Table 15. Link Budget Analysis

It is known that

$$\text{P(dBm)}= 10\log\left(\frac{Pin\ \text{watts}}{1\text{x}10^{-3}}\right).\text{[Ref19]} \tag{28}$$

This means that the power at the output of the BCP 400 is equal to-1.25dBm . For the first channel with interferometer #M3b the total power to reach the receiver is given by

$$-1.25\text{dBm}-30.0\text{dB}= -31.25\text{dBm}. \tag{29}$$

For the second channel with interferometer #M9c the power at the receiver is given by

$$-1.25\text{dBm}-27.0\text{dB}= -28.25\text{dBm}. \tag{30}$$

For the third channel with interferometer #M8b the power at the receiver is

$$-1.25\text{dBm}-27.9\text{dB}= -29.15\text{dBm}. \tag{31}$$

The values for power at the receiver for each channel are also tabulated in Table 15.

C. TESTING AND EVALUATION

In Chapter III the general design considerations for the Mach-Zhender interferometers are discussed. In Figure 16 an ideal normalized transfer function is illustrated for a Mach-Zhender interferometer. It depicts only fourteen folds of the interferometer's folded output. The additional folds beyond these fourteen are not of use because they start to trail off towards extinction. In Figure 17 the axis of Figure 16 has been scaled to illustrate the #6 and #7 folds of the normalized transfer function. The actual #6 and #7 folds are used below to tune the interferometers. In this section the actual design specifications and characteristic waveforms are obtained and detailed.

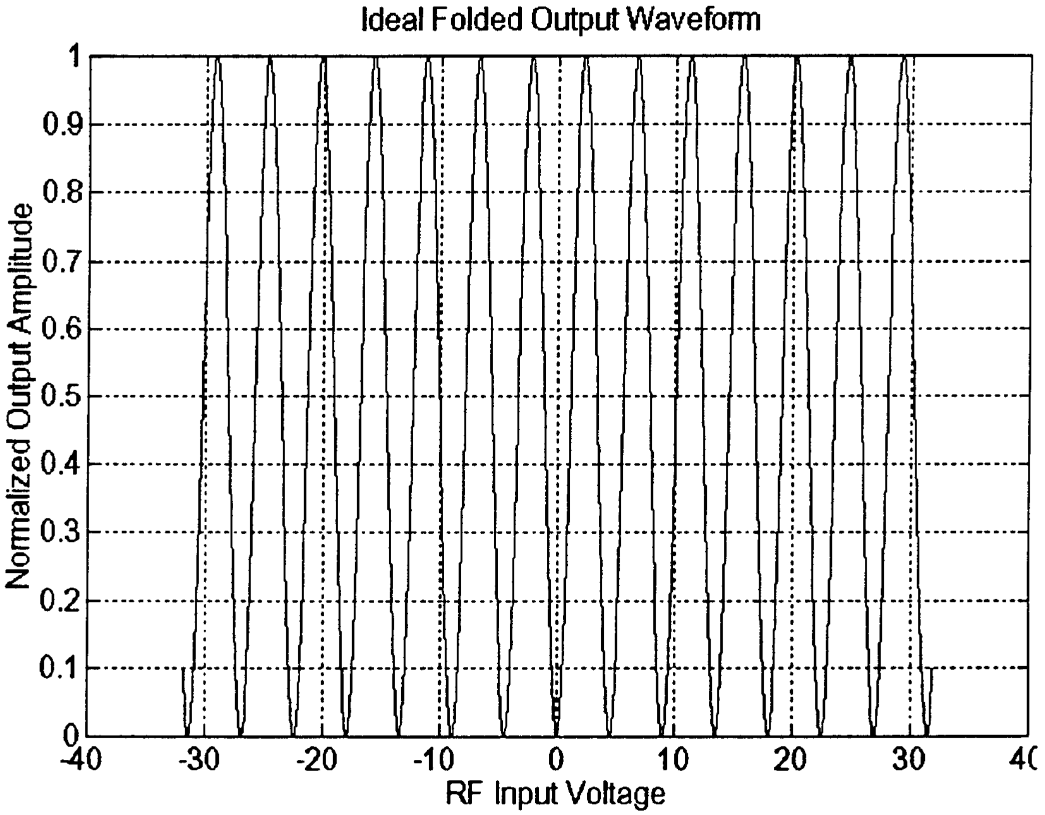


Figure 16. Ideal Normalized Transfer Function Of MZI

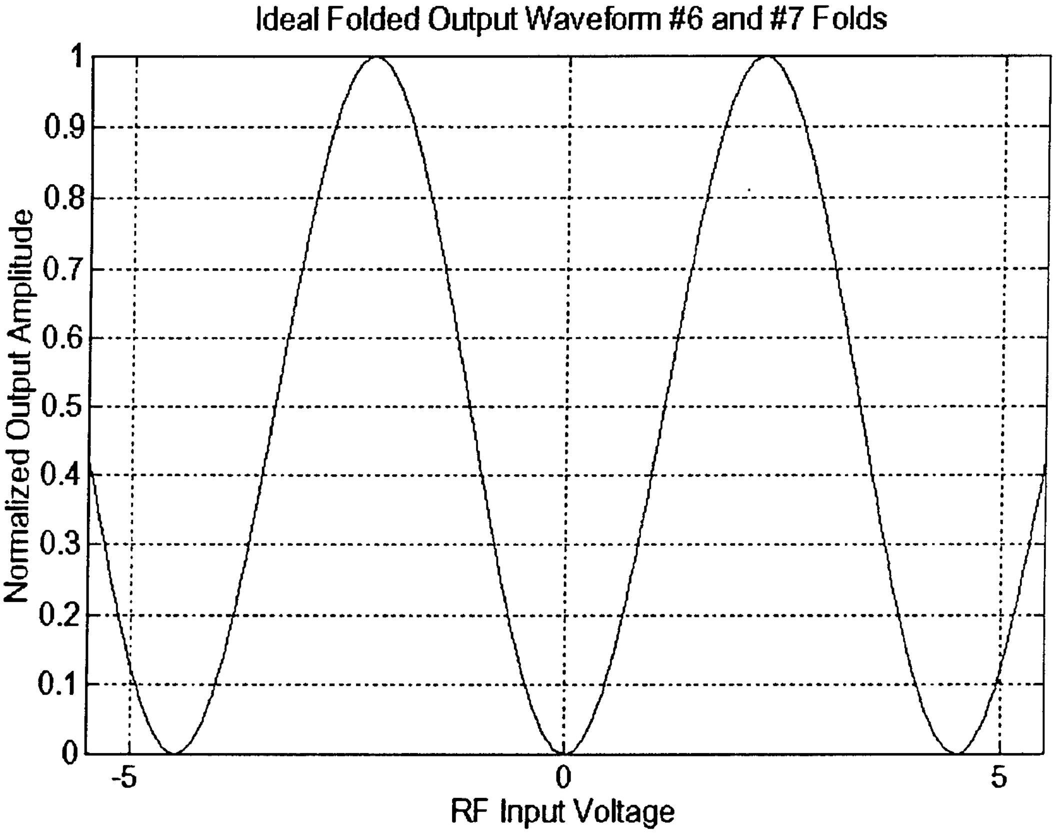


Figure 17. #6 and #7 Folds Of Ideal Normalized MZI Transfer Function

1. Tuning and Performance of the Interferometers

The first step in tuning the interferometers is to determine the exact V_π of each device. This is accomplished by ramping the input RF voltage across each of the interferometers so that a series of folds are visible for analysis. V_π is obtained by measuring the voltage between the minimum and maximum of a fold. By measuring the voltage between the adjacent minima of a fold, one cycle, $2V_\pi$ is obtained. This process is illustrated in Figure 18 for the Modulus 9 interferometer, identification # M3b.

In Figure 18 there are two waveforms in two different windows. The top waveform is the triangle wave RF input voltage to the interferometer that provides the ramped voltage. The bottom waveform is the series of detected folds due to the ramped RF input. This display is obtained with a Tektronix RTD720A Real Time Digitizer. In the display, V1 is the voltage level of Cursor #1, V2 is the voltage level of Cursor #2, t1 and t2 are the time values for cursors one and two respectively, DV is the difference in voltage levels between Cursor #1 and #2, and Dt is the difference in time between the two cursors.

The RTD720A allows the cursor to be moved to the same data point in each window. This allows the first cursor to be moved to a maximum of a fold in the second window and then be repositioned to the first window at the same data point. The second cursor is then placed at the next minimum of a fold and then is repositioned to the same data point in the first window. Notice that in Figure 18 Cursor #1 has been positioned on the maximum of a fold in the second window and is then moved to its corresponding position directly above in the first window. Cursor #2 likewise has been positioned on the next minimum of a fold in the second window and then is repositioned to its corresponding position directly above in the first window. Now, DV indicates the difference in voltage levels between the two cursors which equals V_π. V_π for this interferometer, identification #M3b, is measured as 2.25 V. This same method with the RTD720A is used to obtain the V_π for each of the remaining interferometers. Figure 19 depicts the measurement of V_π for the second interferometer, identification #M9c. From

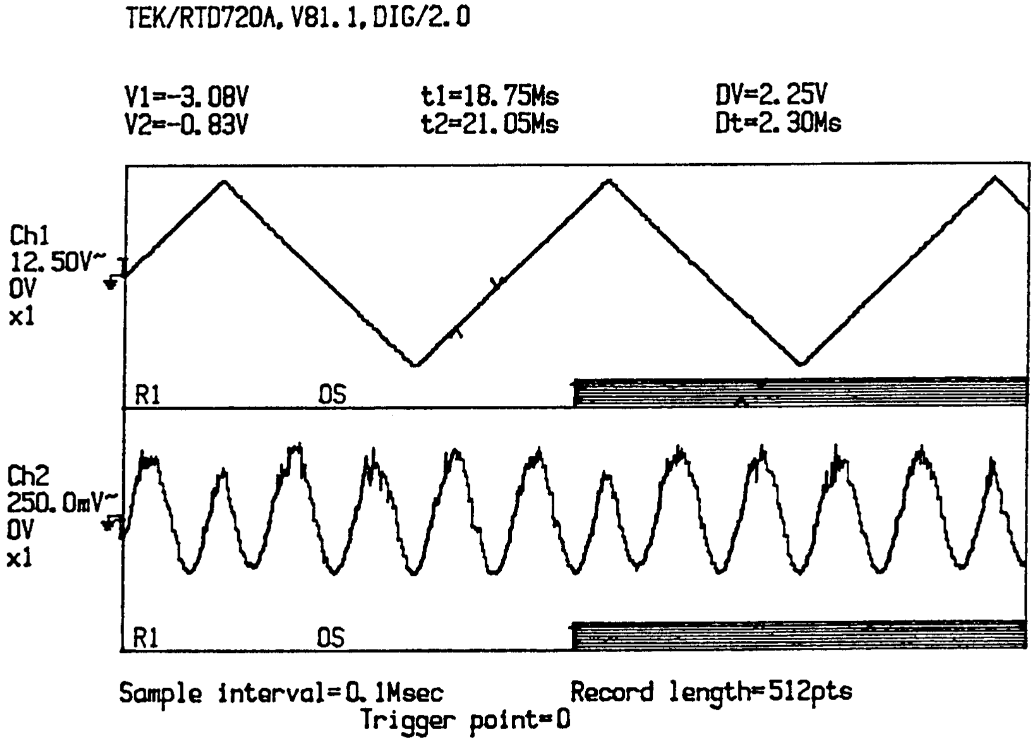


Figure 18. Measurement of Vpie For Interferometer #M3b

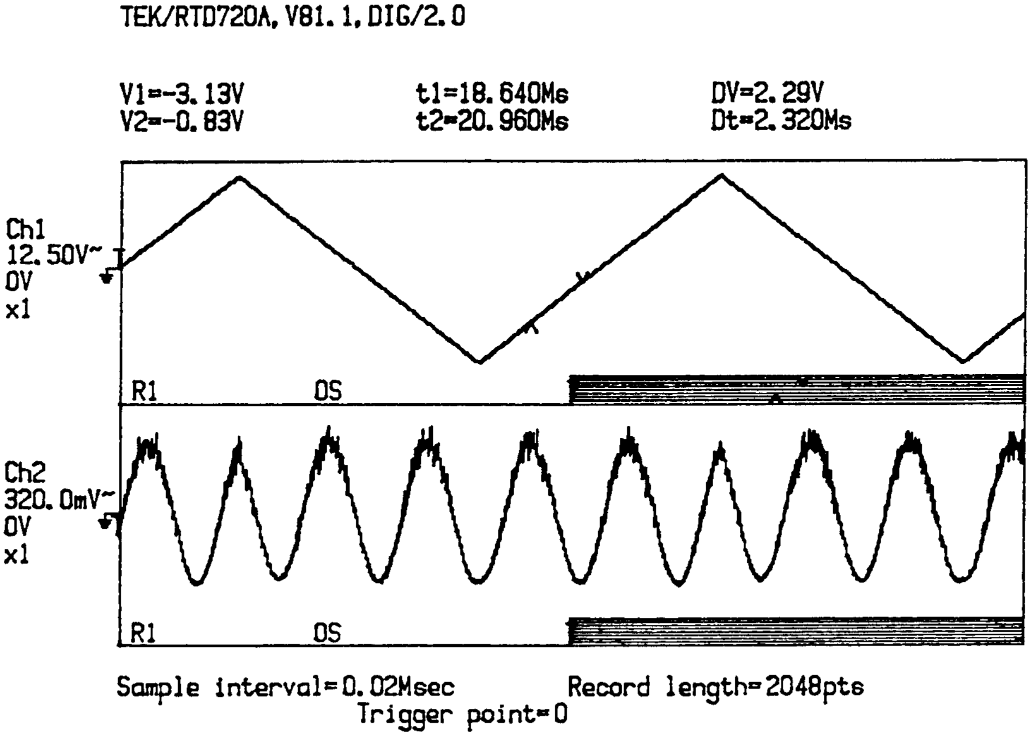


Figure 19. Measurement of Vpie For Interferometer #M9c

this figure, V_π=2.29V for this device. Figure 20 shows the measurement of V_π for the third interferometer in the system design, identification #M8b. From this figure, V_π=2.29V for this device.

Next, the system design is referenced to the Modulus 9 interferometer, device #M3b. The number of folds required by the 8-bit system is determined by using the V_π obtained for the Modulus 9 interferometer. For this device V_π=2.25V.

Using the same formulas discussed in Chapter III, the number of folds required is given by

$$F_{req} = \frac{2^B-1}{2m_{\min}} = \frac{2^8-1}{(2)(9)} = \frac{255}{18} = 14.17. \tag{32}$$

The least significant bit in volts is given by

$$V_{LSB} = \frac{V_\pi}{m_{\min}} = \frac{2.25V}{9} = 250mV. \tag{33}$$

It is known that one complete fold is $2V_\pi$ and that

$$2V_\pi = 2m_i V_{LSB}. \tag{34}$$

This implies that

$$2(2.25V) = 2(9)V_{LSB} \tag{35}$$

and

$$4.5V = 18V_{LSB} \tag{36}$$

which means that a complete fold takes 4.5V and is divided up into 18 slots of 250 mV each. It is also known from the discussion in Chapter III that

$$F_{req} = \frac{2^B-1}{2m_{\min}} < \frac{V_{\max}}{V_\pi}. \tag{37}$$

From this equation $V_{\max}$is obtained as

$$V_{\max} = 14.1667(2.25V) = 31.875V. \tag{38}$$

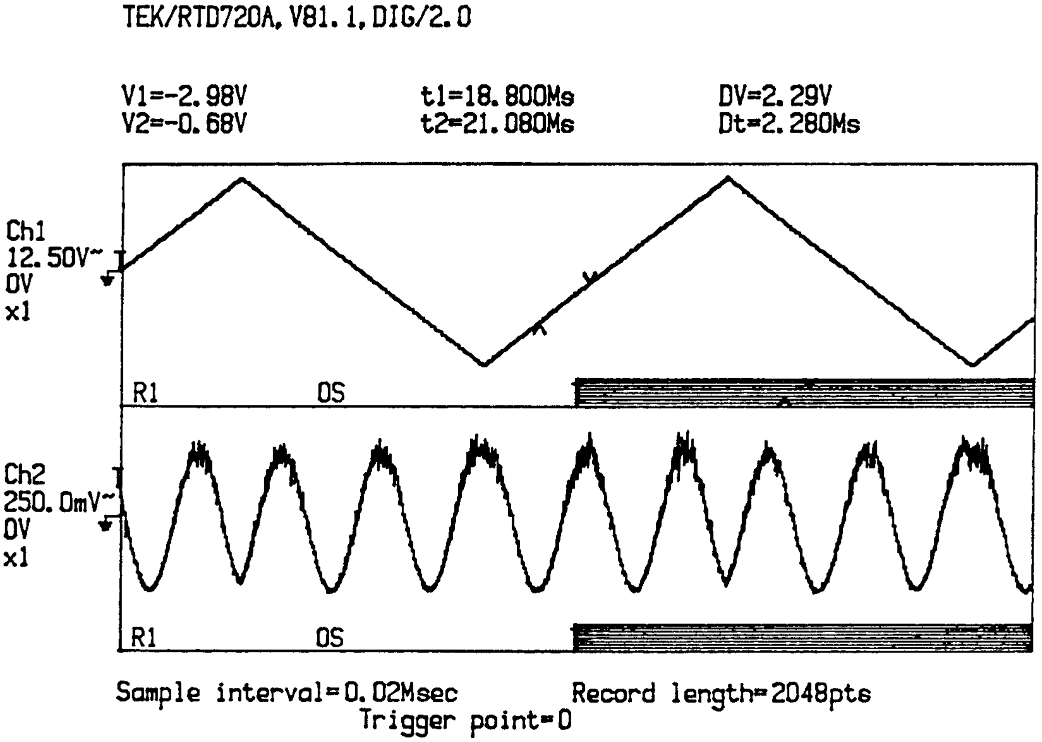


Figure 20. Measurement of Vpie For Interferometer #M8b

V_{min} is just $-V_{max}$, therefore $V_{min} = -31.875V$.

For the 8-bit system design the difference in voltage between V_{min} and V_{max} needs to be divided up into a comparator ladder with 255 steps each having a step size of 250 mV. The first voltage level is at $V_{min} = -31.875V$. A staircase (ADC transfer function) is formed between V_{min} and V_{max} with 255 steps each having a step size of 250 mV. Figure 21 depicts a portion of this staircase indicating the principle discussed here.

Just as the comparator ladder begins at V_{min} and ends at V_{max} likewise the corresponding Modulus 9 interferometer transfer function with 14.17 folds needs to start at V_{min} and end at V_{max}. This is accomplished by applying a DC bias to the RF input of the interferometer through the Bias-Tee. The DC bias enables the curve to be shifted so that the minimum of the first fold is exactly at $V_{min} = -31.875V$. Or, since we know that $V_\pi=2.25V$ which corresponds to one half-cycle and $2V_\pi=4.50V$ which corresponds to one full cycle, the interferometer transfer function can be shifted using any minimum point of the folded waveform. This method is used to apply the DC bias to the Modulus 9 folded waveform.

The minimum point of the #7 fold is chosen as the DC adjustment point for simplicity of scaling with the RTD720A. Since $V_{min} = -31.875V$ and one folding period equals $2V_\pi=4.5V$, this implies that when the input RF voltage is set at

$$-31.875 + 7(4.5) = -375mV, \tag{39}$$

the #7 fold of the folded waveform should be at a minimum. Figure 22 illustrates this adjustment for the Modulus 9 interferometer.

In Figure 22 Cursor #1 is in window #1 at the voltage closest to -375 mV. V1 reads 0.39V. Cursor #2 is moved to the same data point in window #2. This is where the #7 fold minimum should be. The DC bias is adjusted until the #7 fold minimum lines up with Cursor #2. Once lined up the folded waveform is in the correct alignment and the DC Bias is recorded and set. In this case the DC bias is 2.64V.

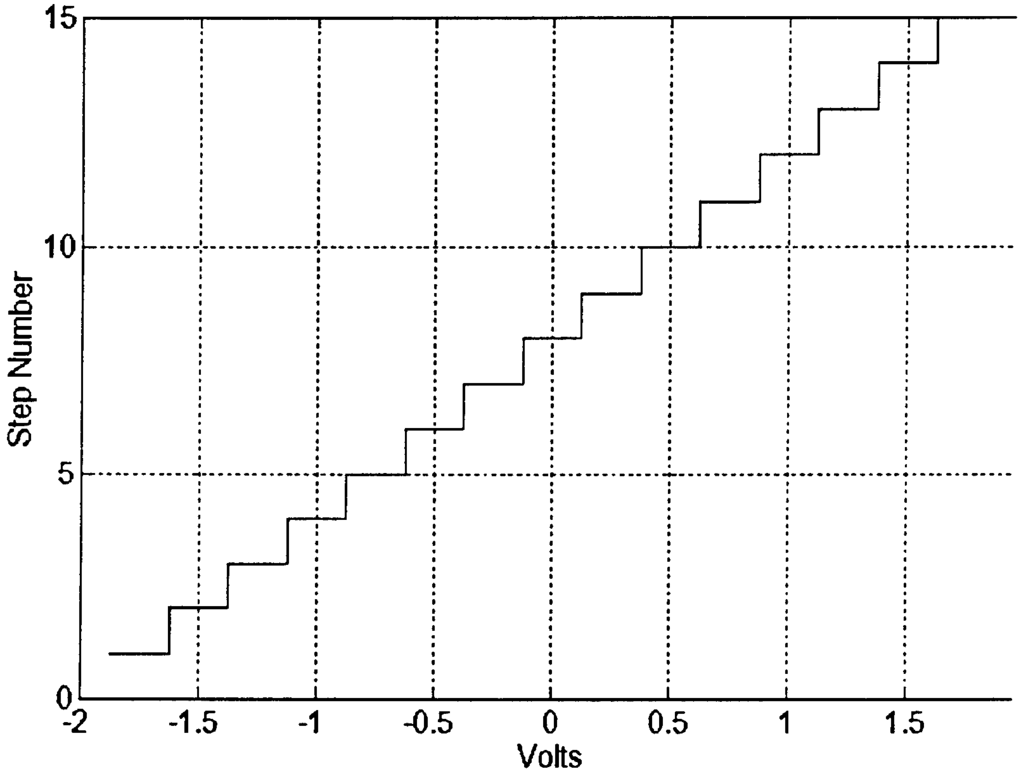


Figure 21. Comparator Ladder With 250 mV Step-Size

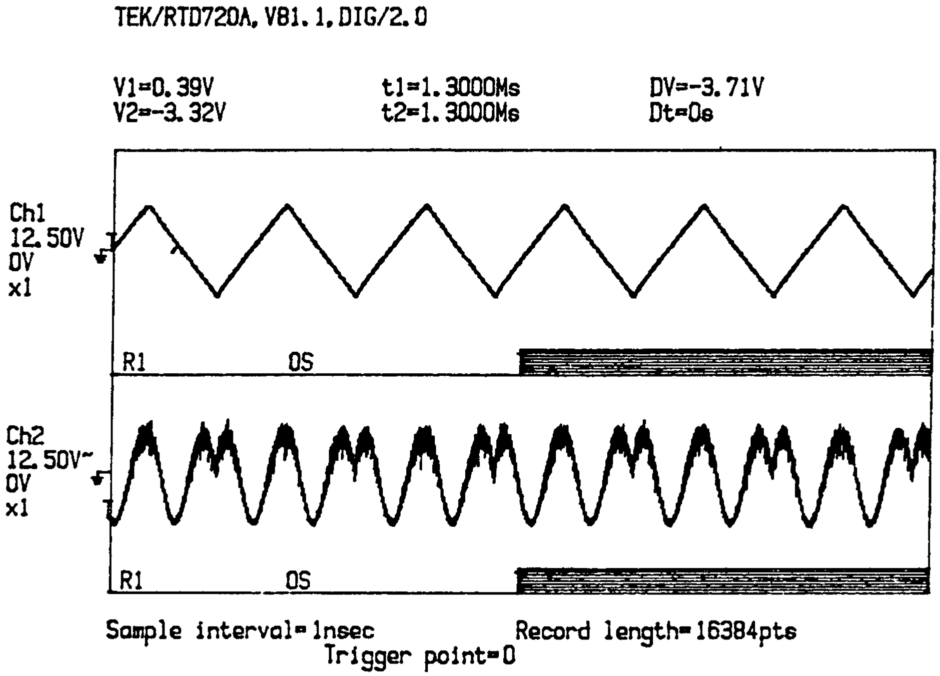


Figure 22. Modulus 9 DC Offset Adjustment

The process for tuning the Modulus 10 interferometer is similar to tuning the Modulus 9 interferometer with the addition of adjusting the Modulus 10 V_π referenced to the Modulus 9 V_π. The number of folds required is given by

$$F_{req} = \frac{2^B-1}{2(m)} = \frac{2^8-1}{2(10)} = \frac{255}{20} = 12.75V. \tag{40}$$

The voltage for V_π is determined from the least significant bit voltage formula

$$V_{LSB} = \frac{V_\pi}{10} \rightarrow V_\pi = 10(250mV) = 2.5V. \tag{41}$$

To set the V_π for the Modulus 10 interferometer the RF attenuator is adjusted while the RTD720A is used to measure the period of the folded waveform. The higher the attenuation the greater the period of the waveform. In Figure 23 the RF attenuation is set for the Modulus 10 interferometer. Cursor #1 and #2 are set in the second window so that Cursor #1 is at a minimum of a fold and Cursor #2 is one-half period away at the next maximum. The cursors are then moved to their corresponding data points in the first window and DV is measured. This process is repeated until DV=V_π=2.5V or as close to 2.5 V as possible. In this case DV=2.49V.

Next, the DC bias must be set to make the folded waveform start at V_{min}=-31.875V. The same method of applying a DC bias is used for the Modulus 10 waveform as is discussed above with the Modulus 9 waveform. The minimum point of the #6 fold is chosen as the DC adjustment point for simplicity of scale. Since V_{min}=-31.875V and one folding period equals $2V_\pi$=2(2.5V)=5.0V, this implies that when the input RF voltage is set at

$$-31.875 + 6(5) = -1.875V, \tag{42}$$

the #6 fold of the folded waveform should be at a minimum. Figure 24 illustrates this adjustment for the Modulus 10 interferometer.

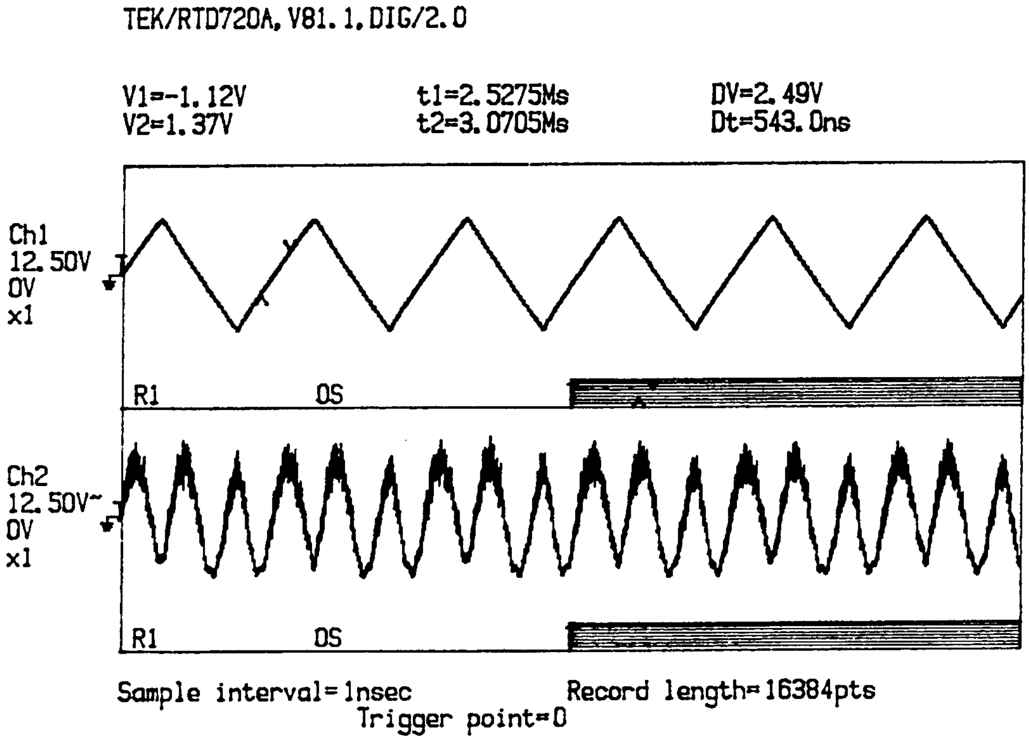
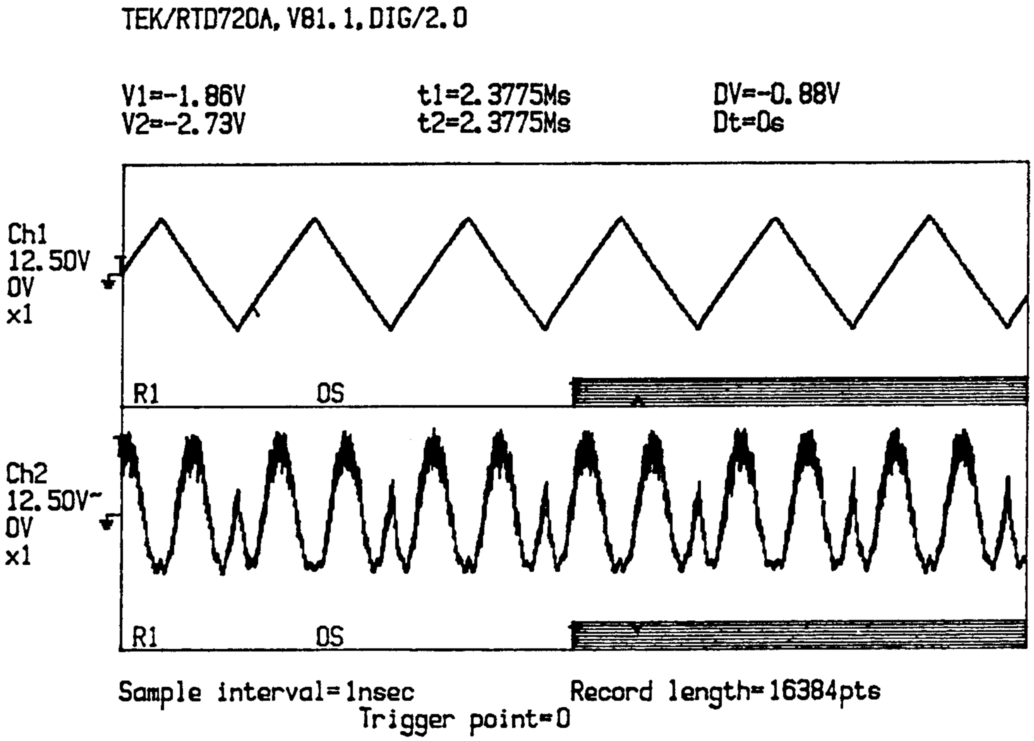


Figure 23. Modulus 10 RF Attenuation Adjustment



```
TEK/RTD720A, V81.1, DIG/2.0

V1=-1.86V          t1=2.3775Ms          DV=-0.88V
V2=-2.73V          t2=2.3775Ms          Dt=0s

Sample interval=1nsec          Record length=16384pts
                  Trigger point=0
```

Figure 24. Modulus 10 DC Offset Adjustment

In Figure 24 Cursor #1 is in window #1 at the voltage closest to -1.875V. V1 reads -1.86V. Cursor #2 is moved to the same data point in window #2. This is where the #6 fold minimum should be. The DC bias is adjusted until the #6 fold minimum lines up with Cursor #2. Once lined up the folded waveform is in the correct alignment and the DC Bias is recorded as 0.519V and is set.

The process for tuning the Modulus 11 interferometer is exactly the same as described above with the Modulus 10 interferometer. First, the Modulus 11 V_π must be referenced to the Modulus 9 V_π. The number of folds required is given by

$$F_{req} = \frac{2^{B}-1}{2(m)} = \frac{2^{8}-1}{2(11)} = \frac{255}{22} = 11.59. \tag{43}$$

The voltage for V_π is determined from the least significant bit voltage formula given by

$$V_{LSB} = \frac{V_\pi}{m} = \frac{V_\pi}{11} \rightarrow V_\pi = 11(250mV) = 2.75V. \tag{44}$$

To set the V_π for the Modulus 11 interferometer the RF attenuator is adjusted while the RTD720A is used to measure the period of the folded waveform. The higher the attenuation the greater the period of the waveform. In Figure 25 the RF attenuation is set for the Modulus 11 interferometer. Cursor #1 and #2 are set in the second window so that Cursor #1 is at a minimum of a fold and Cursor #2 is one-half period away at the next maximum. The cursors are then moved to their corresponding data points in the first window and DV is measured. This process is repeated until DV=V_π=2.75V or as close to 2.75 V as possible. In this case DV=2.73V.

Next, the DC bias must be set to make the folded waveform start at V_{min}=-31.875V. The same method of applying a DC bias is used for the Modulus 11 waveform as is discussed above with the Modulus 9 waveform. The minimum point of the #6 fold is chosen as the DC adjustment point for simplicity of scale. Since V_{min}=-31.875V and one folding period equals $2V_\pi$=2(2.75V)=5.50V, this implies that when the input RF voltage is set at

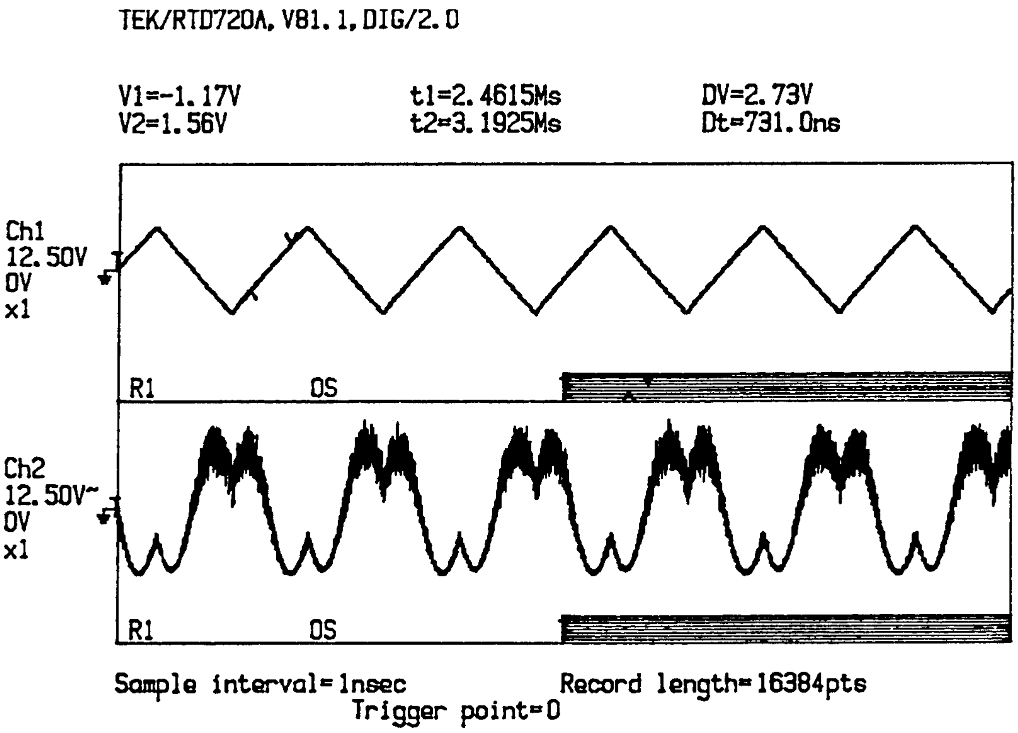


Figure 25. Modulus 11 RF Attenuation Adjustment

$$-31.875 + 6(5.50V) = 1.125V, \tag{45}$$

the #6 fold of the folded waveform should be at a minimum. Figure 26 illustrates this adjustment for the Modulus 11 interferometer.

In Figure 26 Cursor #1 is in window #1 at the voltage closest to 1.125V. V1 reads 1.12V. Cursor #2 is moved to the same data point in window #2. This is where the #6 fold minimum should be. The DC bias is adjusted until the #6 fold minimum lines up with Cursor #2. Once lined up the folded waveform is in the correct alignment and the DC Bias is recorded as 0.303V and is set. Table 16 summarizes the RF attenuation and DC Bias settings for each interferometer.

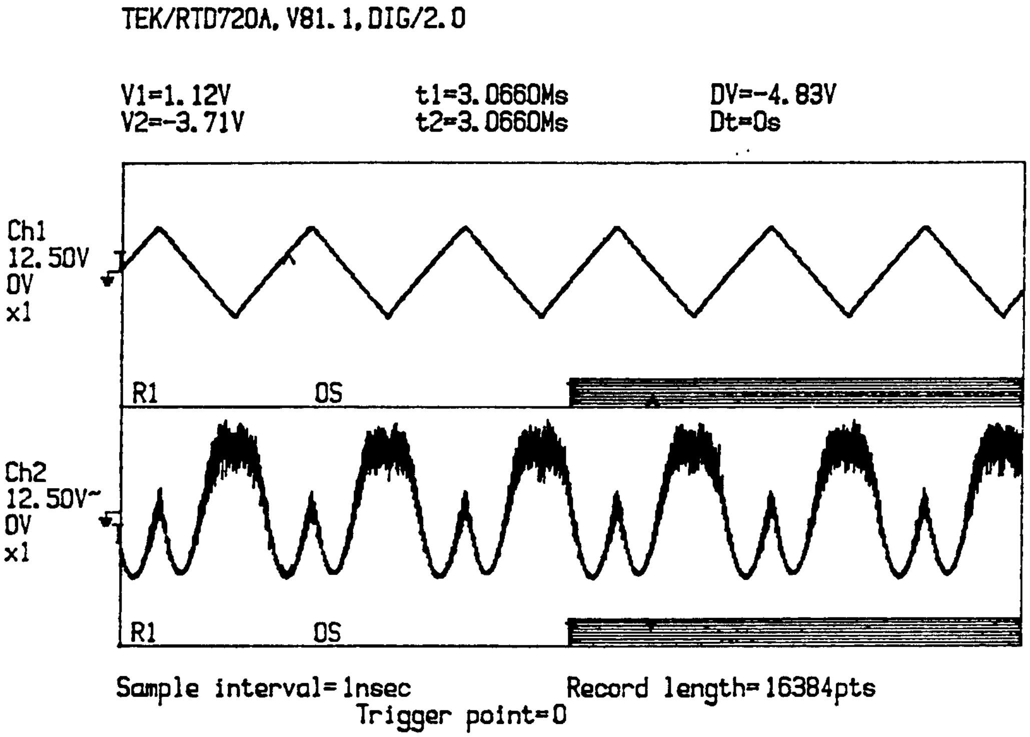
Interferometer #	RF Attenuation Setting	DC Bias Setting
M3d	0 dB	2.64V
M9c	2.0 dB	0.519V
M8b	6.1 dB	0.303V

Table 16. RF Attenuation And DC Bias Summary

2. Characteristic Waveforms/System Performance

In Chapter III a method is given to obtain the characteristic waveforms for each interferometer using LabVIEW. This section discusses another method of obtaining the interferometer characteristic waveforms using the RTD720A Real Time Digitizer.

The waveforms are obtained in the lab by first providing a ramp voltage input to the interferometer. The voltage ramps between -35V and 35V. The ramp voltage is supplied by a triangle waveform generated with the Wavetek 142 Signal Generator. This triangle wave is then amplified by a Tektronix AM501 Operational Amplifier to get the range needed. The amplified triangle wave is then connected to a 1X4 RF splitter which divides the RF energy into four even outputs. Three channels are used to send the triangle



TEK/RTD720A, V81.1, DIG/2.0

V1=1.12V t1=3.0660Ms DV=-4.83V
V2=-3.71V t2=3.0660Ms Dt=0s

Sample interval=1nsec Record length=16384pts
Trigger point=0

Figure 26. Modulus 11 DC Offset Adjustment

wave to each of the three interferometers. The fourth channel is used to send the signal to the RTD720 Real Time Digitizer via a Tektronix A6902B Isolator. The Isolator is necessary to divide the RF signal by approximately 10 so that the signal is within the range of the RTD720A . The divide by 10 scale is used on the isolator but this is only an approximation. An accurate conversion factor is necessary to measure the input.

The conversion factor is determined by taking the output from the splitter into the 1 MΩ termination of the Tektronix 2445B Oscilloscope and measuring the triangle wave with the automatic measuring feature of the scope. This is measured as 66.3 V peak-to-peak. Next, the output from the splitter is connected to the 50 Ω termination of channel one on the RTD720A and is again measured. The triangle wave now exhibits a voltage of 296.8 mV peak-to-peak. Therefore the conversion factor for the measurement of the triangle wave with the RTD720A is given by

$$\frac{296.8mV}{66.3V} = \frac{4.48mV}{V}. \tag{46}$$

To obtain the characteristic waveforms of each interferometer, channel one of the RTD720A is selected to display the triangle waveform input to the interferometers. Channel two is selected to display the output of the Modulus 9 interferometer after the optical signal has passed through the BCP310A Optical Receiver and has been amplified by the HP8347 wideband amplifiers. Figure 27 illustrates the setup for obtaining the interferometer characteristic waveforms with the RTD720A Real Time Digitizer. Figure 28 illustrates the input RF triangle wave in window #1 and the characteristic waveform of the Modulus 9 interferometer. Likewise Figure 29 and Figure 30 illustrate the triangle wave in window #1 and the interferometer characteristic waveforms of the Modulus 10 and Modulus 11 interferometers in window #2 respectively. Figure 31 illustrates the Modulus 9, Modulus 10, and Modulus 11 characteristic waveforms, without any RF attenuation or DC Bias applied, together from top to bottom respectively.

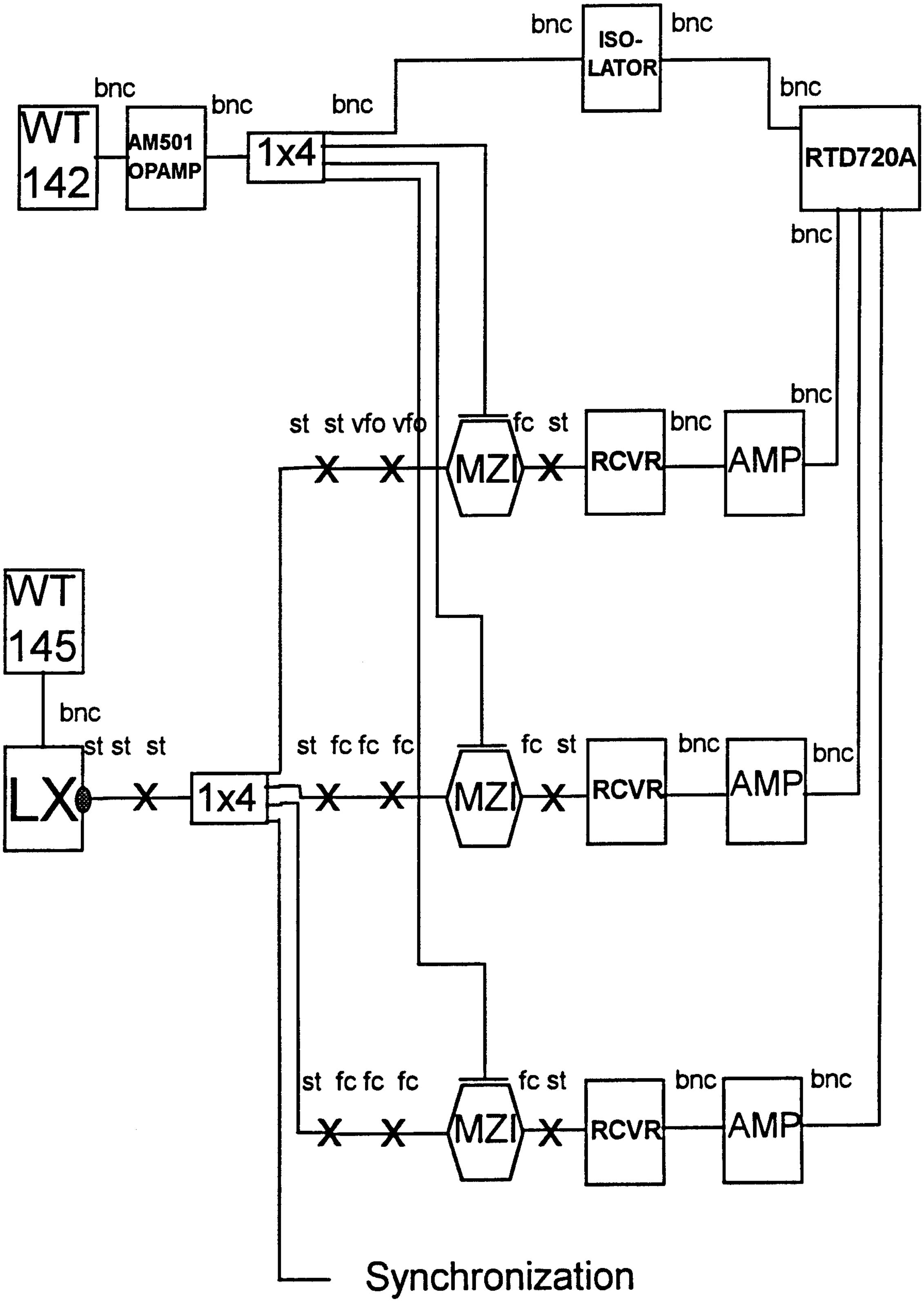


Figure 27. Setup For Obtaining Characteristic Waveforms With The RTD720A

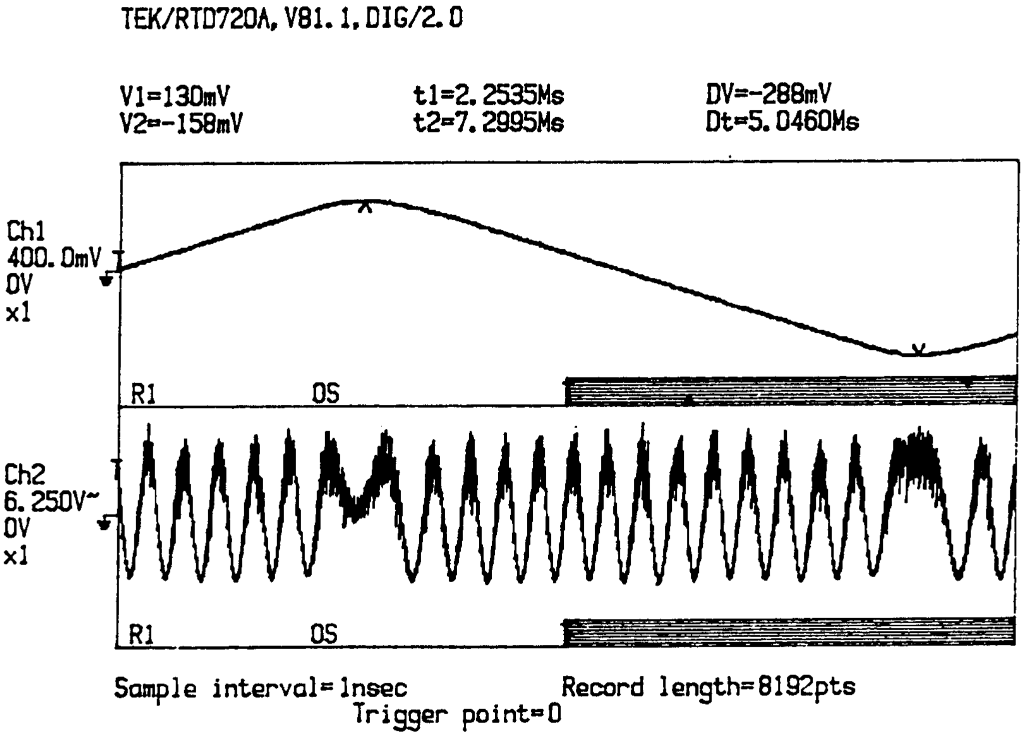


Figure 28. Modulus 9 Characteristic Waveform

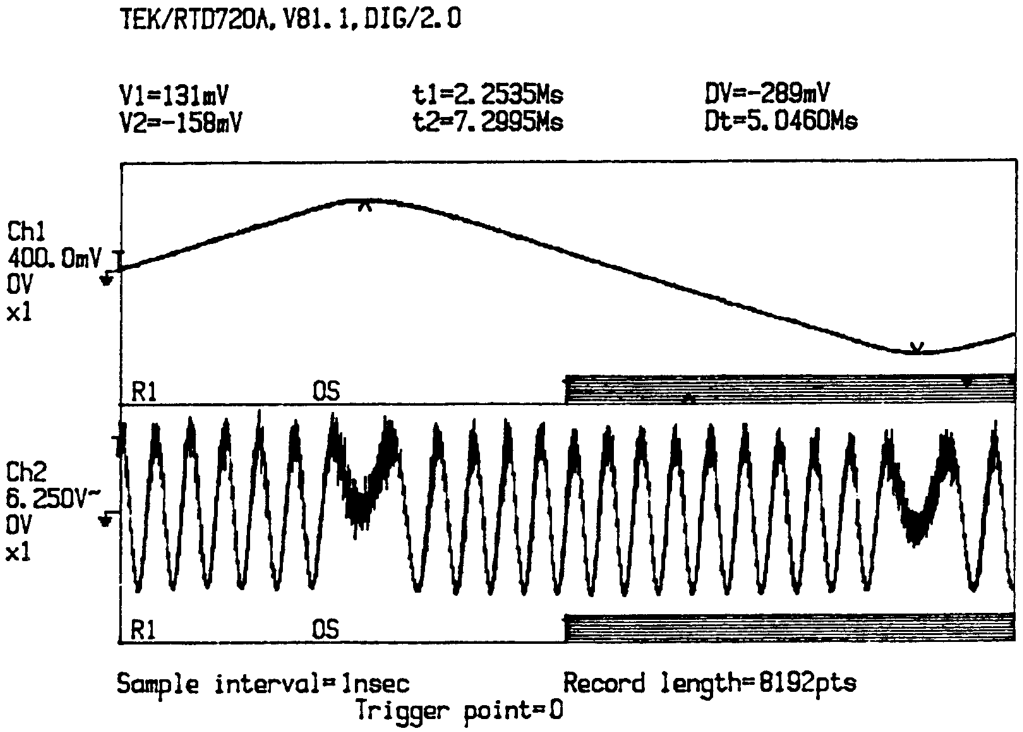


Figure 29. Modulus 10 Characteristic Waveform

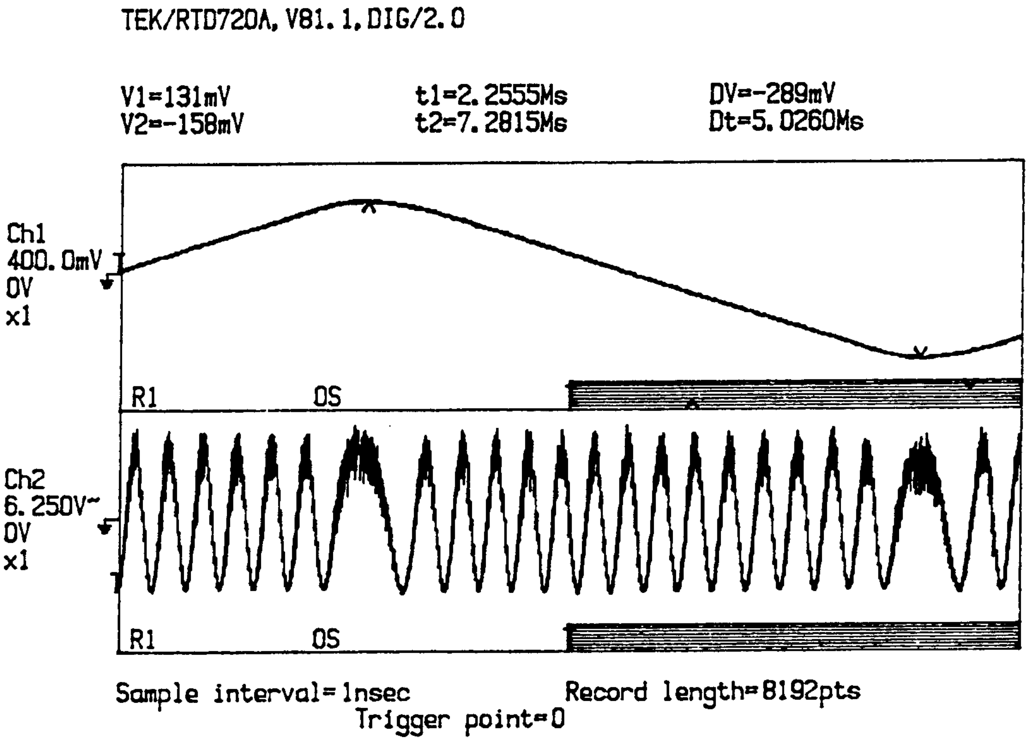


Figure 30. Modulus 11 Characteristic Waveform

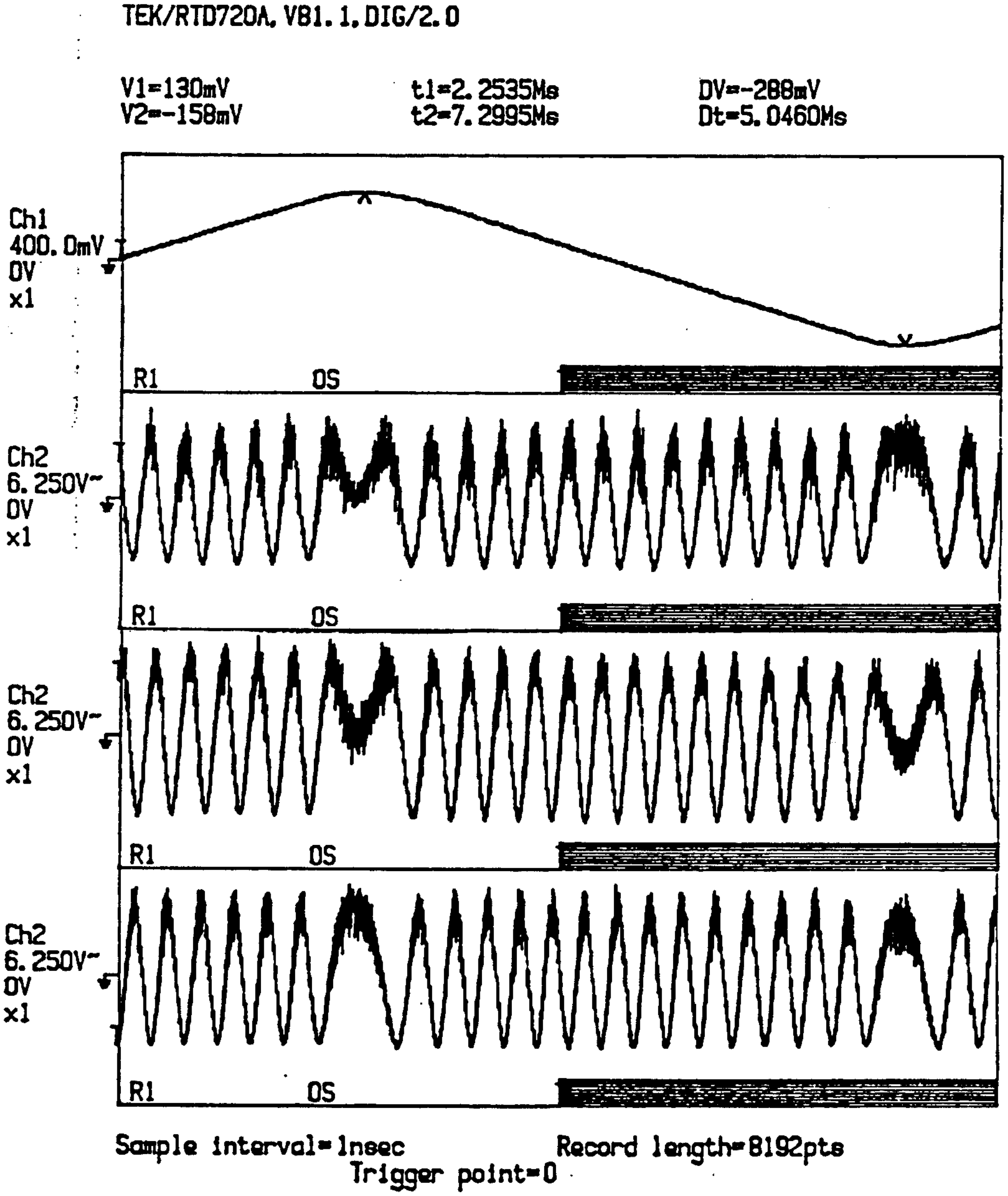


Figure 31. Modulus 9, Modulus 10, and Modulus 11 Characteristic Waveforms

D. INTERFACE WITH BOARDS

In order to provide the circuit boards with a pulsed input, the BCP400 Laser Transmitter is pulsed with a 20 ns square wave at its digital input. This produces a 20 ns square wave at the output of the BCP400 Laser Transmitter. This output is sent through a single-mode 1X4 splitter. Three of the splitter's outputs are connected to the Modulus 9, Modulus 10, and Modulus 11 inputs respectively. The fourth channel coming out of the 1X4 splitter is used for synchronization with the boards. After the light travels through each of the interferometers it passes through a BCP310A Optical Receiver followed by a HP8347 wideband receiver. After the folded waveform signal is amplified it is sent to the circuit boards for SNS encoding. The 8-bit optical system diagram is repeated in Figure 32 for reference.

To illustrate a pulsed output in Figure 33, a sinusoid waveform is input to the RF input of the interferometers and the BCP400 Laser Transmitter is driven by a 20 ns digital pulse. The sinusoid waveform is converted into a folded wave output by each of the interferometers. Figure 33 displays the sinusoid RF input in window #1 and one interferometer pulsed folded wave output in window #2. This type of pulsed output is then sent to the circuit boards for encoding and analysis.

The optical SNS folding circuit design is ready to be interfaced with the Modulus 9, Modulus 10, and Modulus 11 circuit boards. Two other thesis students are continuing this research work.

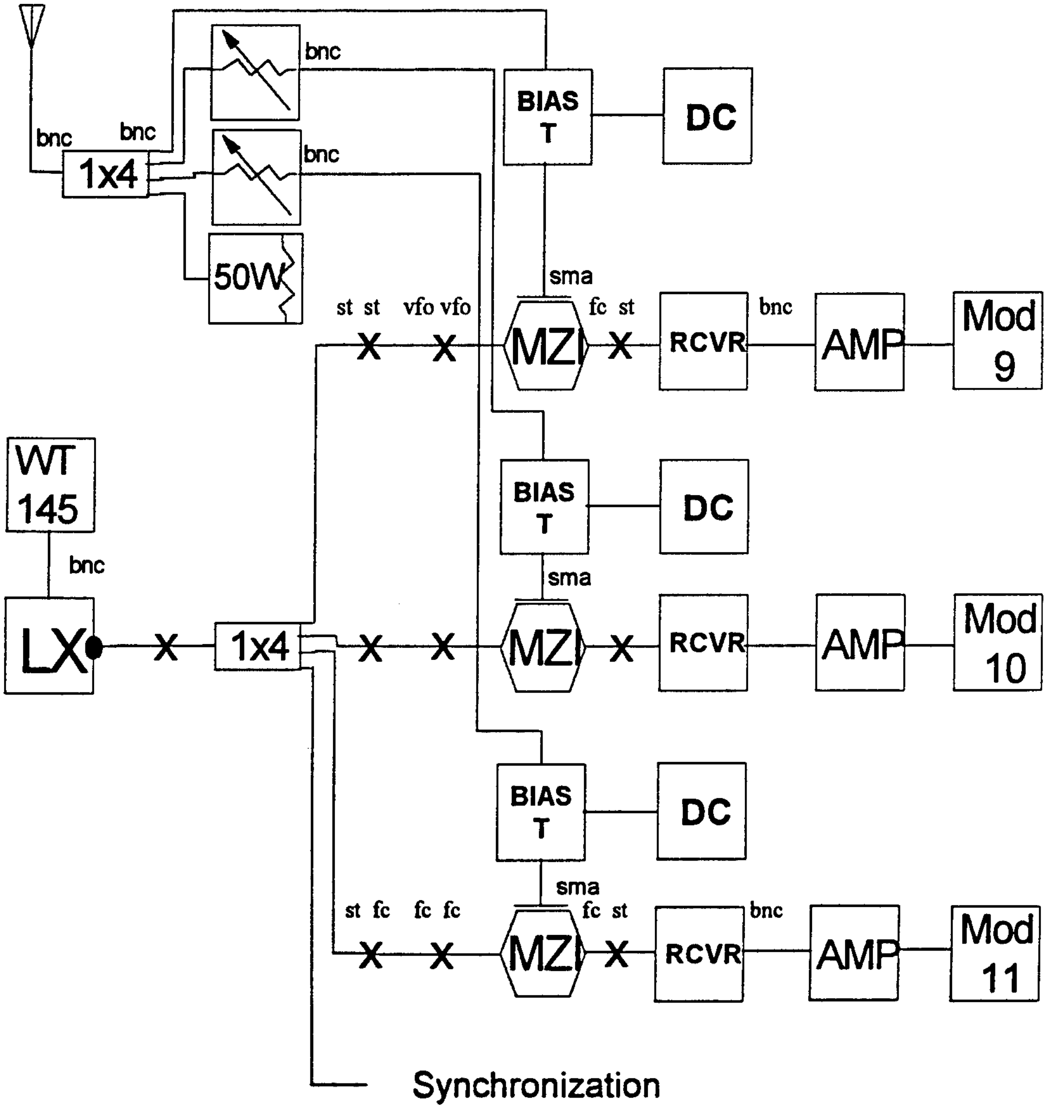


Figure 32. 8-Bit Optical System Diagram

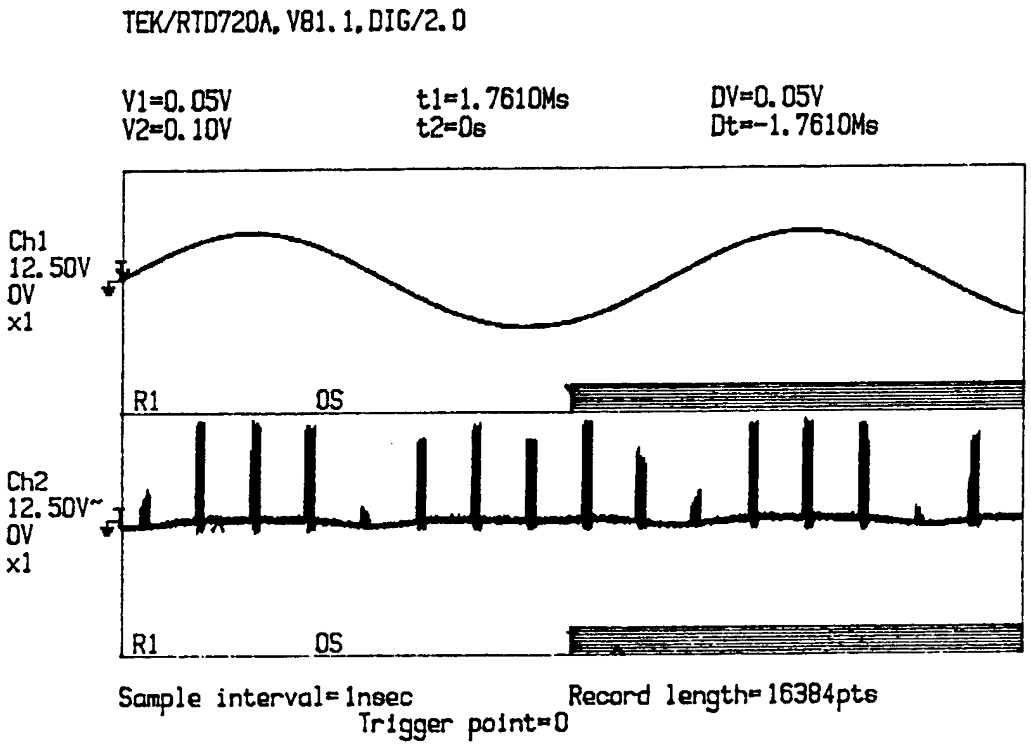


Figure 33. Sinusoid RF Input With Folded Waveform Output

V. SUMMARY

This thesis detailed the design of an 8-bit optical SNS folding circuit to be used as the front end of an electro-optical analog-to-digital converter. The 8-bit 5 MHz SNS ADC is near completion. All digital boards are built and are currently being tested and integrated with the optical processor front end designed in this thesis. Preliminary testing and evaluation of the optical front end are performed in Chapter IV.

The end goal of this thesis effort was to build an 8-bit optical SNS folding circuit to function as the front end of an electro-optical analog-to-digital converter. These objectives have been accomplished using the available materials and components as detailed.

APPENDIX A. LABVIEW DESIGN

To continue with the simultaneous development of the circuit boards and optical system, the initial programs [Ref. 8] need enhancement to provide the following features:

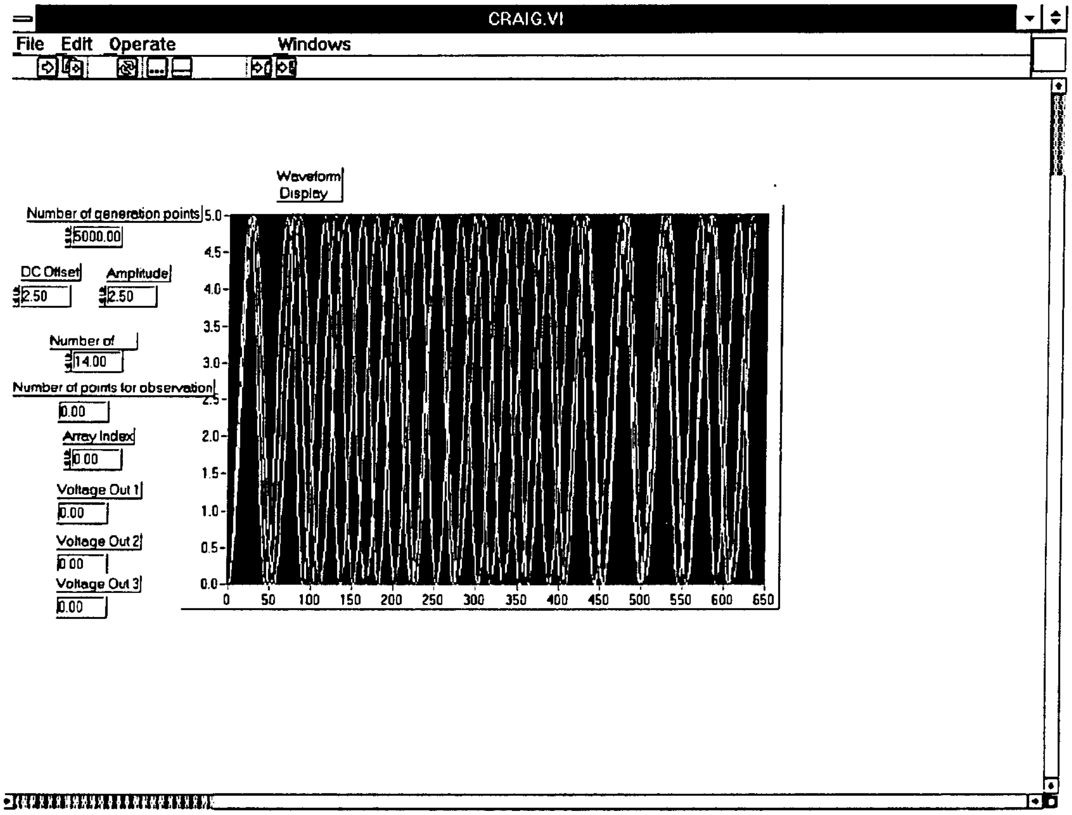
1. Output the array data to an output file for analysis and printing.
2. Automate the system to provide array output from start to finish without having to manually index the array.
3. Provide an external trigger to automate data collection at the HP1631D Logic Analyzer.
4. Provide a voltage ramp output to drive one Mach Zender Interferometer.
5. Collect the word data (ie. eight bits from the word + 1 bit parity) from the Analog-to-Digital Converter within LabVIEW for analysis and printing. This step automates the data collection.

A. EXTENDED DEVELOPMENT OF LABVIEW VI'S

The enhancement of the initial programs [Ref. 8] started by renaming JEFFSTEP.VI, to CRAIG.VI. The front panel and diagram for this VI are displayed in Figure 34 and Figure 35 respectively. From this file the design is done in increments from CRAIG.VI through CRAIG8.VI. Each successive design attempts to add a new feature to the VI. The new file is tested and evaluated and the process repeats with each new design.

1. Array Data Output and Automation

Files named CRAIG1.VI through CRAIG3.VI experiment with different possible designs to automate the output of the array. CRAIG4.VI is the result, see Figure 36. This VI automates the array output so that the array index no longer has to be manually advanced at the control panel. The voltages are set to change within the for loop every one second. The voltage outputs are supplied to the Modulus 9, Modulus 10, and



Number of generation points: 5000.00

DC Offset: 2.50

Amplitude: 2.50

Number of: 14.00

Number of points for observation: 0.00

Array Index: 0.00

Voltage Out 1: 0.00

Voltage Out 2: 0.00

Voltage Out 3: 0.00

Figure 34. Front Panel Display of CRAIG.VI

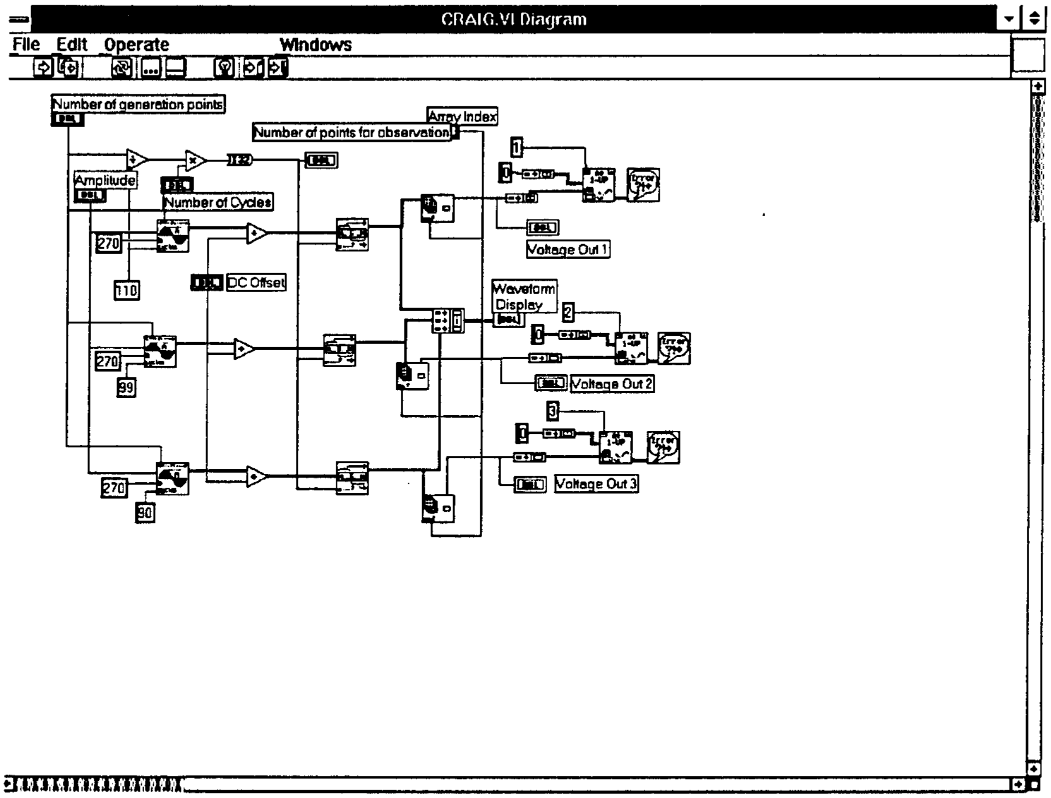


Figure 35. Diagram Display of CRAIG.VI

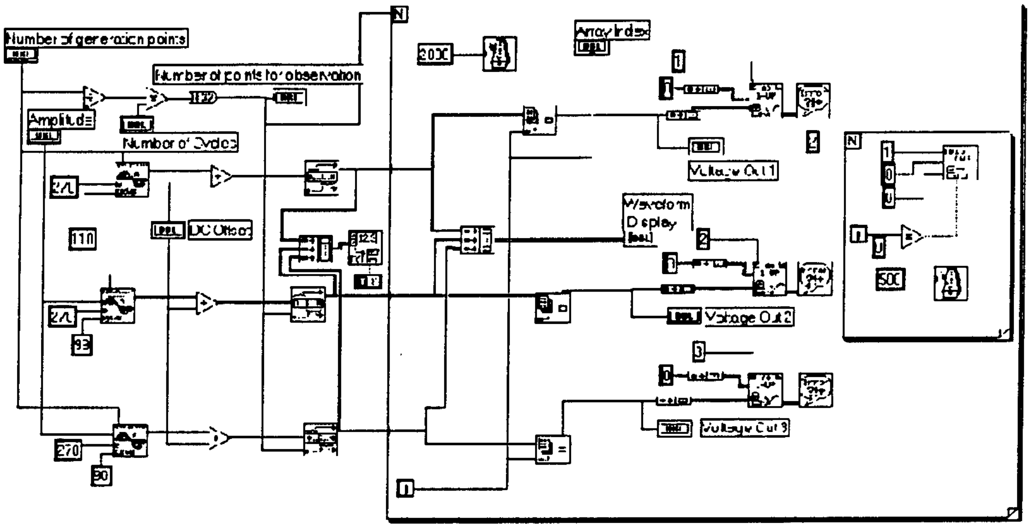


Figure 36. Diagram Display of CRAIG4.VI

Modulus 11 boards at DAC0 out, pin number 20. In addition , in CRAIG4.VI, the array output is written to a spreadsheet file in ASCII text format for later analysis and printing. The array output file is named OUTPUT.TXT.

2. External Trigger

The next step of the design involves the HP1631D Logic Analyzer. The data for each run can be acquired with the HP1631D Logic Analyzer if LabVIEW generates an external trigger. Using the write to digital line VI in LabVIEW, a loop drives the output pin on the Modulus 9 board, pin number 25 high then low. The trigger loop is within the array loop (a nested loop structure). The array loop executes every one second setting the voltages at the Modulus 9, Modulus 10, and Modulus 11 boards. The nested trigger loop executes 0.5 seconds later driving pin 25 high then low. The HP1631D Logic Analyzer is set to trigger on the negative edge of the pulse. The output on pin 25 is a square wave, but it appears very noisy. This has to be corrected in the following designs.

In CRAIG5.VI the noisy trigger output is addressed, refer to Figure 37. The pulse pattern VI replaces the write to digital line VI in the trigger loop . This VI generates a pulse with a set amplitude and width. Again the output is on the Modulus 9 board, pin 25. This design proves less reliable and more noisy in testing than using the write to digital line VI as done previously in CRAIG4.VI. This is not a viable solution to the trigger problem.

In CRAIG6.VI the noisy trigger output is again addressed. A nested sequence structure replaces the nested trigger loop. The array voltage loop is set to execute every

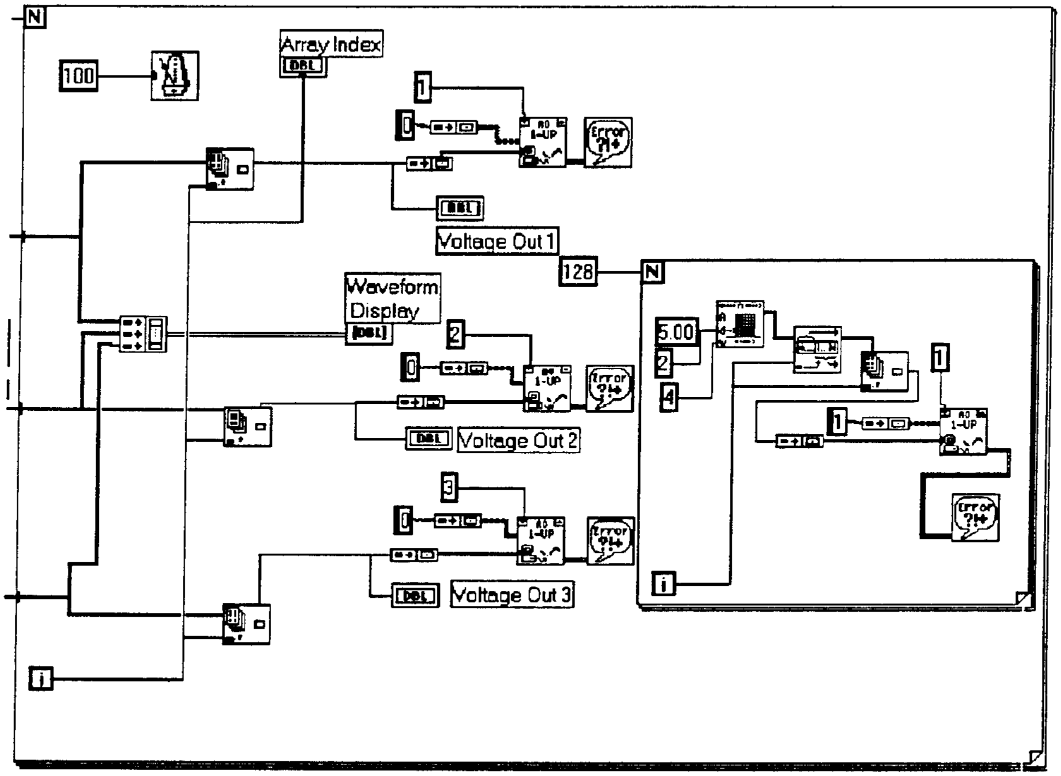


Figure 37. Diagram Display of CRAIG5.VI

second. The sequence structure executes after the waveform voltages within the loop have been set to their respective values. The number "0" sequence executes first. It contains a wait 250 ms (1/4 second) timer that causes a 1/4 second delay before the execution of the next sequence step, refer to Figure 38. The number "1" sequence is executed next. It contains the write to digital line VI driving the output on pin 25 high, see Figure 39. The number "2" sequence executes next. It contains a wait 250 ms timer that causes a 1/4 second delay before the execution of the next sequence step, see Figure 40. The number "3" sequence is executed next. It contains the write to digital line VI driving the output on pin 25 low this time, refer to Figure 41. By adjusting the timers in sequence "0" and sequence "2" the time of the rising and falling edges of the trigger can be adjusted. Note: The trigger must execute within the timing of the loop ie., if the loop is set to execute every one second, the entire time for the trigger cannot exceed one second. This design for the trigger proves to be clean and reliable in testing.

3. Voltage Ramp Output

Next, it is necessary to obtain the transfer functions for each of the three NRL Mach Zender Interferometers. This requires a voltage ramp output from LabVIEW. This is addressed in CRAIG7.VI.

In CRAIG7.VI a loop containing a formula node is added to the system, refer to Figure 42. This loop is outside of the array voltage output loop. The formula node loop generates a normalized ramp voltage with the same number of voltage points for the

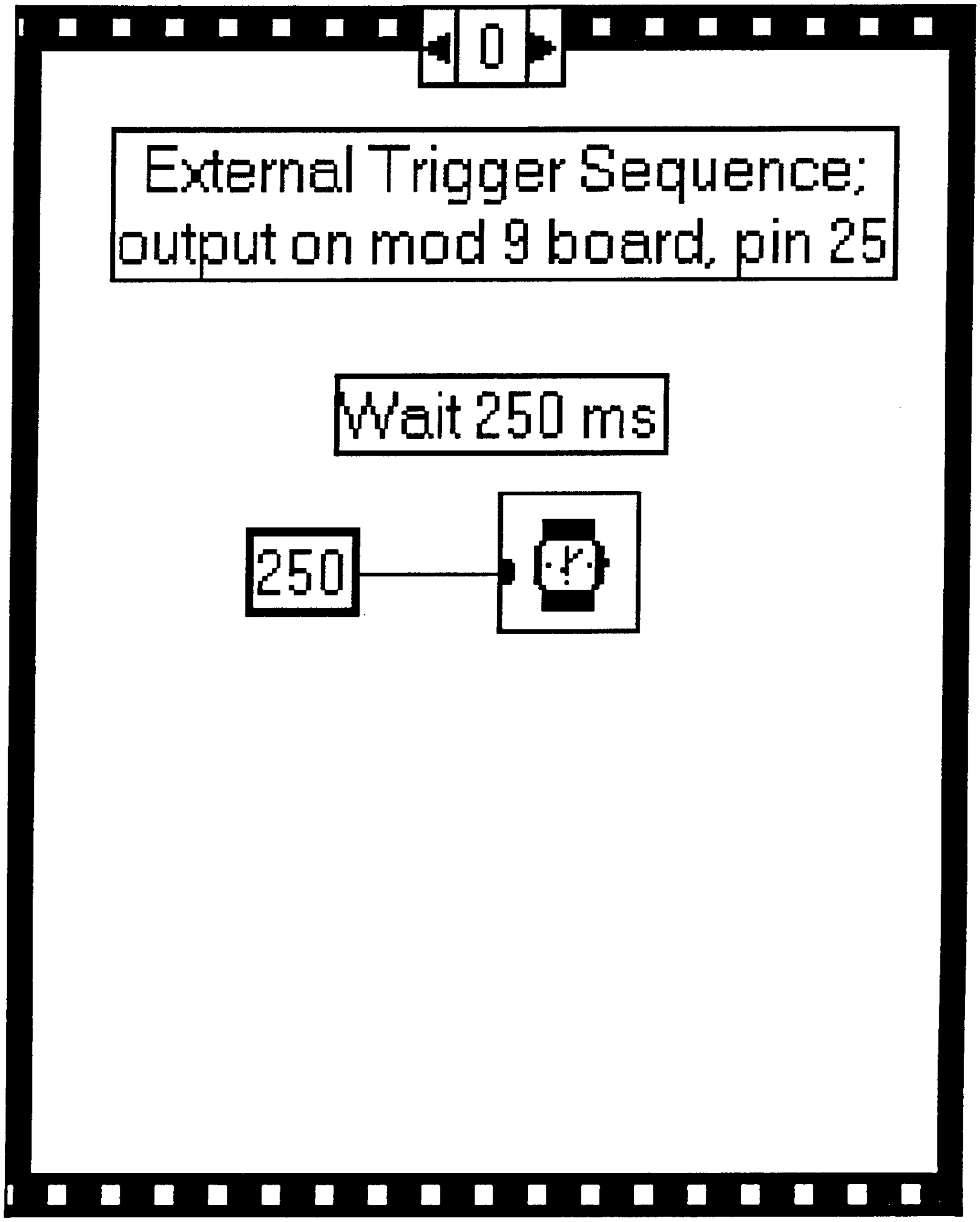


Figure 38. Sequence "0" Structure

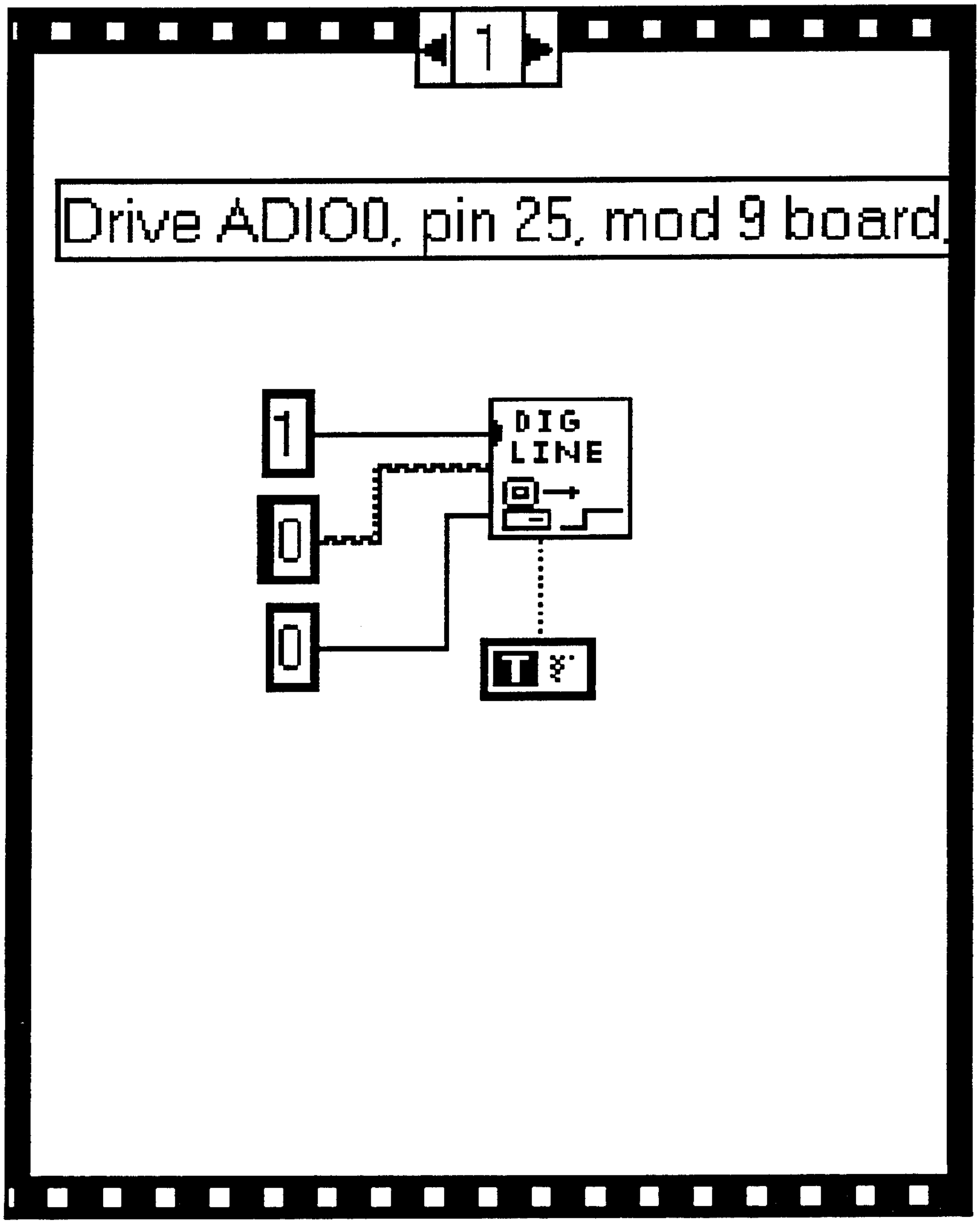


Figure 39. Sequence "1" Structure

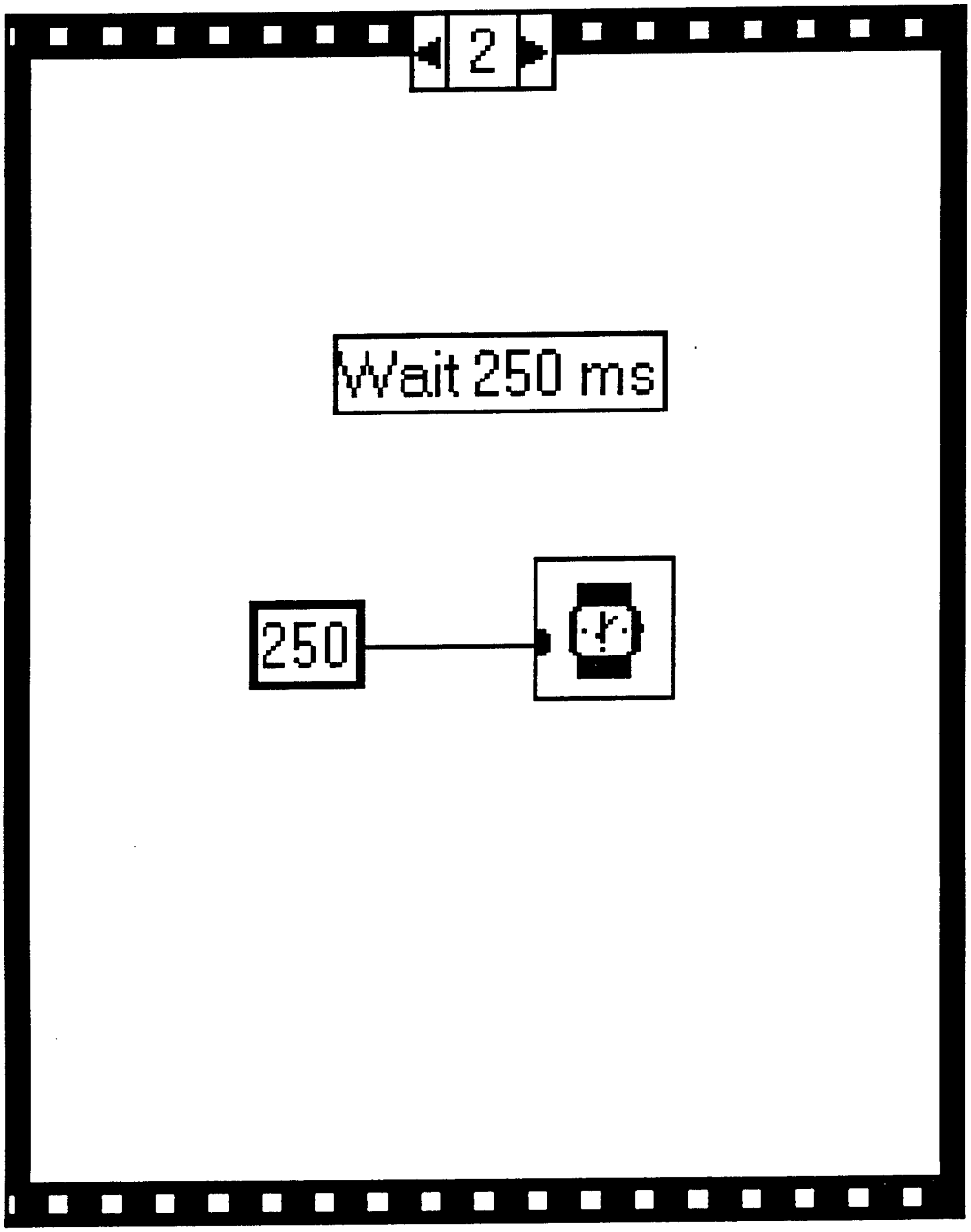


Figure 40. Sequence "2" Structure

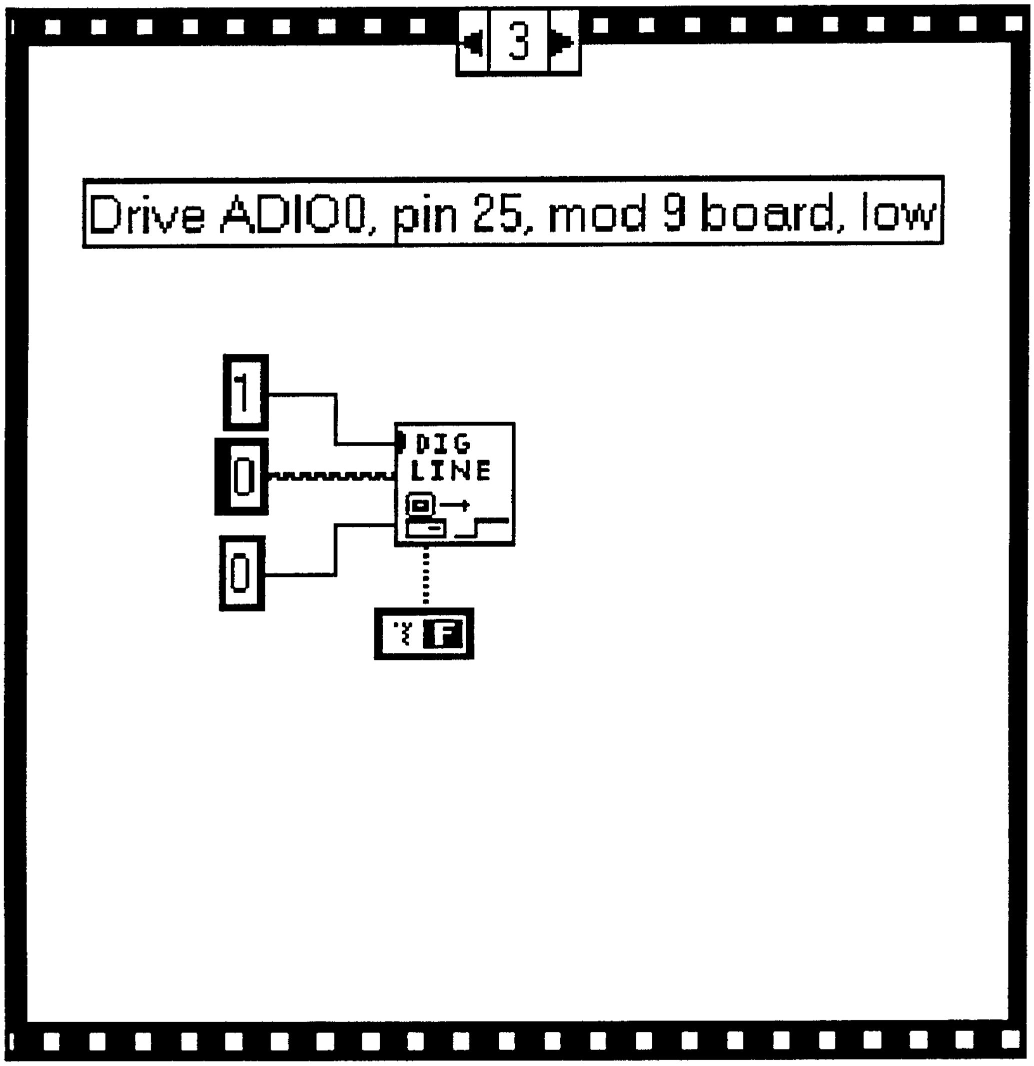


Figure 41. Sequence "3" Structure

interferometer input as the voltage outputs coming from the Modulus 9, Modulus 10, and Modulus 11 boards simulating the folds of the interferometer. The formula within the formula node is listed below:

$$y = \frac{x}{45.5 \times 69.677} \times 2 \times V_\pi . \tag{47}$$

where V_π=2.45V, and x is the point number. The output location for this ramp voltage is on the Modulus 9 board, DAC1 out, pin 21. The ramp output voltage from this formula node is connected to the array output voltages for the Modulus 9, Modulus 10, and Modulus 11 boards and written to the same data output file, OUTPUT.TXT, in the fourth column, for analysis and printing. The ramp voltage input is also displayed on the front panel as "Voltage In 1", see Figure 43. This design allows each interferometer transfer function to be obtained in Chapter III.

4. Automation of Data Collection

The next step in the design involves the limitations of data acquisition with the HP1631D Logic Analyzer. The Logic Analyzer is one of the Lab's older instruments and, as such, has barriers to overcome.

The limitations of the HP1631D Logic Analyzer are listed below:

1. Can only collect up to 1024 data points. If there are more than 1024 data points, the first 1024 points can be collected, then downloaded to the HP disk, then the process must be restarted with data point 1025...etc
2. The HP diskette and text format must be changed through a complex process to obtain an Ascii text file for analysis and printing.

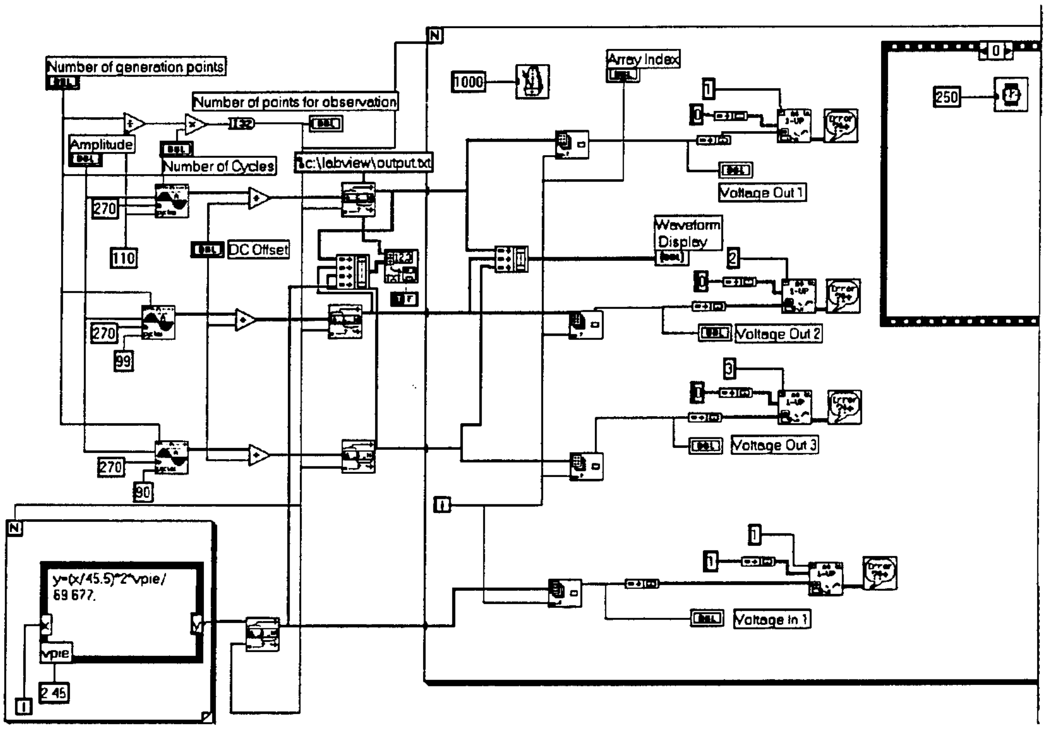
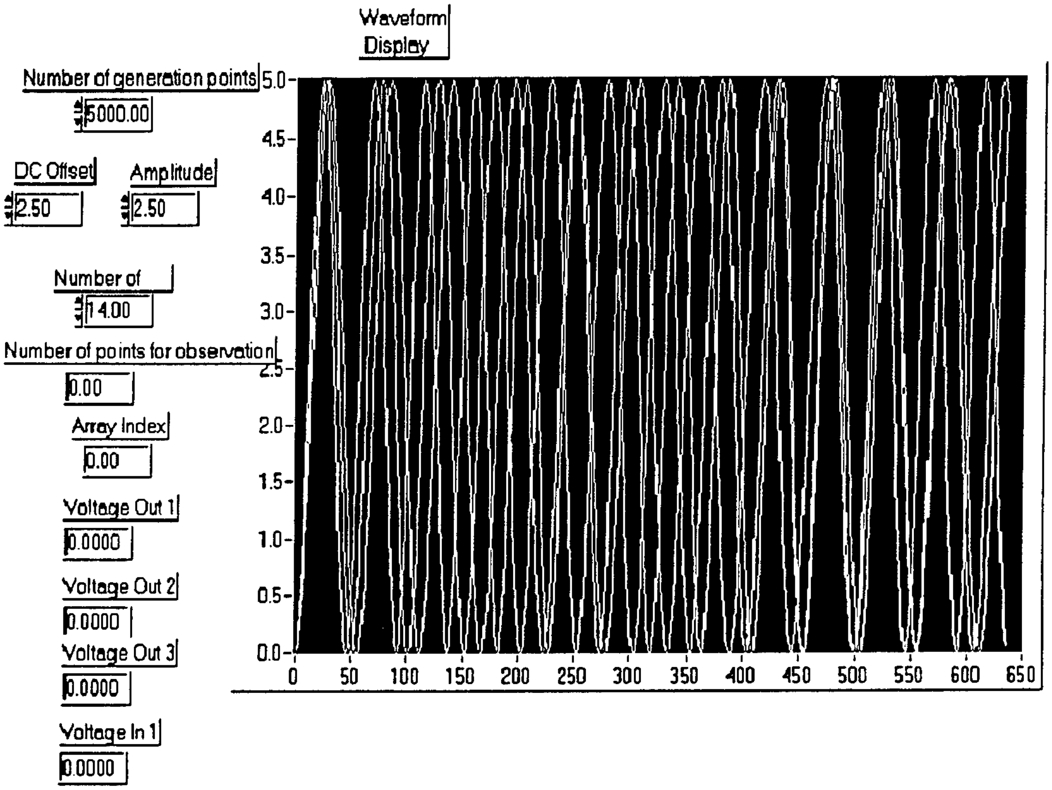


Figure 42. Voltage Ramp Diagram, CRAIG7.VI



Number of generation points 5000.00

DC Offset 2.50

Amplitude 2.50

Number of 14.00

Number of points for observation 0.00

Array Index 0.00

Voltage Out 1 0.0000

Voltage Out 2 0.0000

Voltage Out 3 0.0000

Voltage In 1 0.0000

Figure 43. Front Panel Display, CRAIG7.VI

The complexity of handling the data analysis with the outdated HP system is the reason for wanting data collection and analysis within LabVIEW. This problem is addressed in CRAIG8.VI.

In CRAIG8.VI, a sequence structure for data acquisition is nested within the array output voltages loop. Sequence "0" contains a wait 750 ms (3/4 second) timer that causes a 3/4 second delay before the start of the next step, see Figure 44. Sequence "1" then utilizes the sample channels VI to sample analog input channels on the Modulus 9 board, ACH0-ACH8, pins 3,5,7,9,11,13,15,17, and 4, see Figure 45. The word output is taken from the Analog-to-Digital Converter circuit board in to the pins listed above. The least significant bit is connected to pin 3, the most significant bit to pin 17, and the parity bit to pin 4. For a listing of all pin assignments refer to the AT-MIO-16F I/O connector diagram [Ref. 21]. The write to spreadsheet file VI is also used to write this voltage data to the file, INPUT.TXT. It is then necessary to convert this voltage data to binary format ie., "1" 's and "0" 's. This is accomplished by running the voltages through a comparator bank simulated within LabVIEW, refer to Figure 46. The comparators are located outside of the sequence structure but still within the array output voltages loop. One comparator is used for each bit for a total of nine comparators. Each comparator threshold is set at 2.5 volts. If the voltage taken from the Analog-to-Digital Converter bit is greater than or equal to 2.5 volts a binary "1" is output. If the voltage is less than 2.5 volts a binary "0" is output. This binary word data is then written to a spreadsheet file, WORD.TXT, using the write to spreadsheet file VI, for analysis and printing.

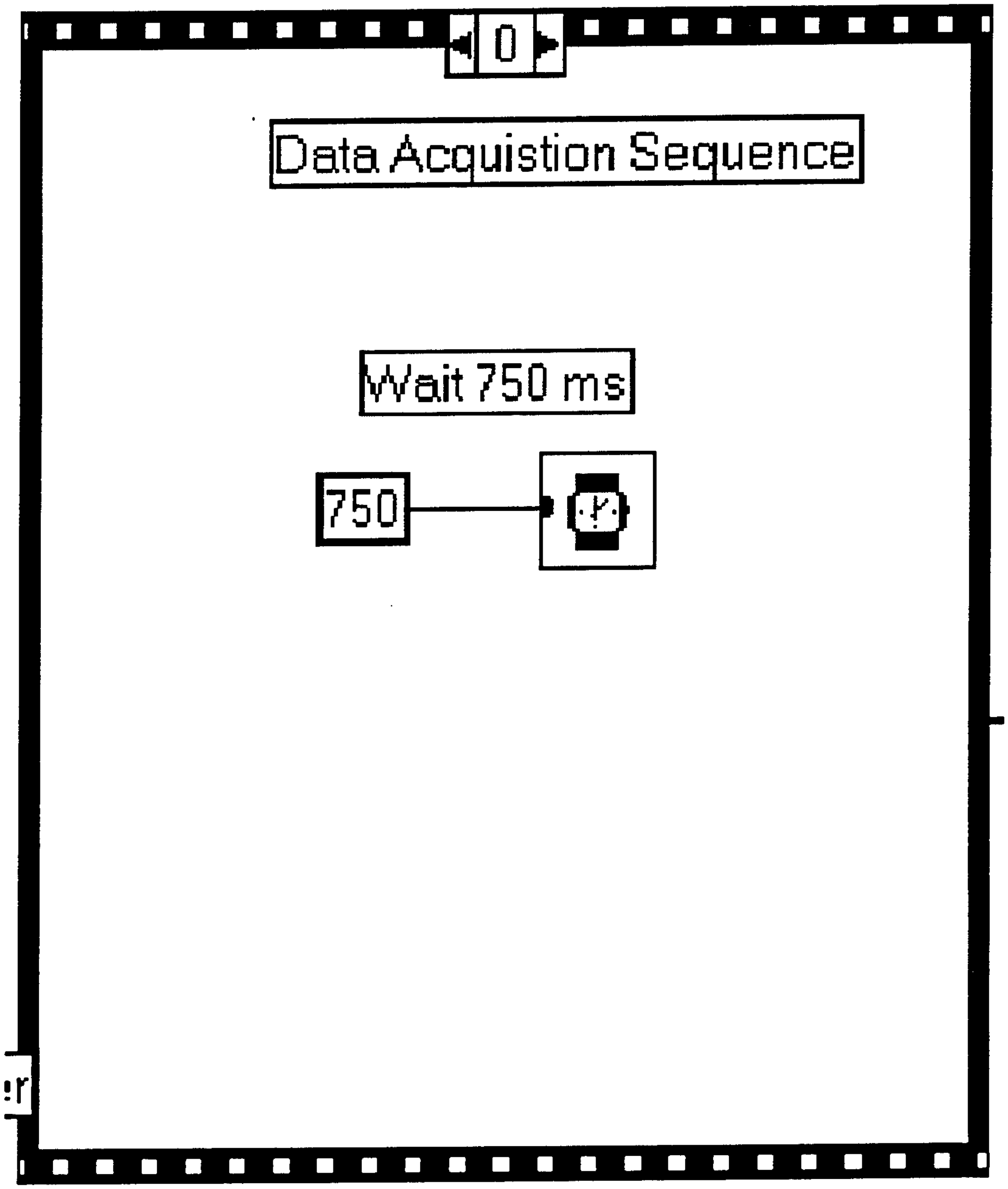
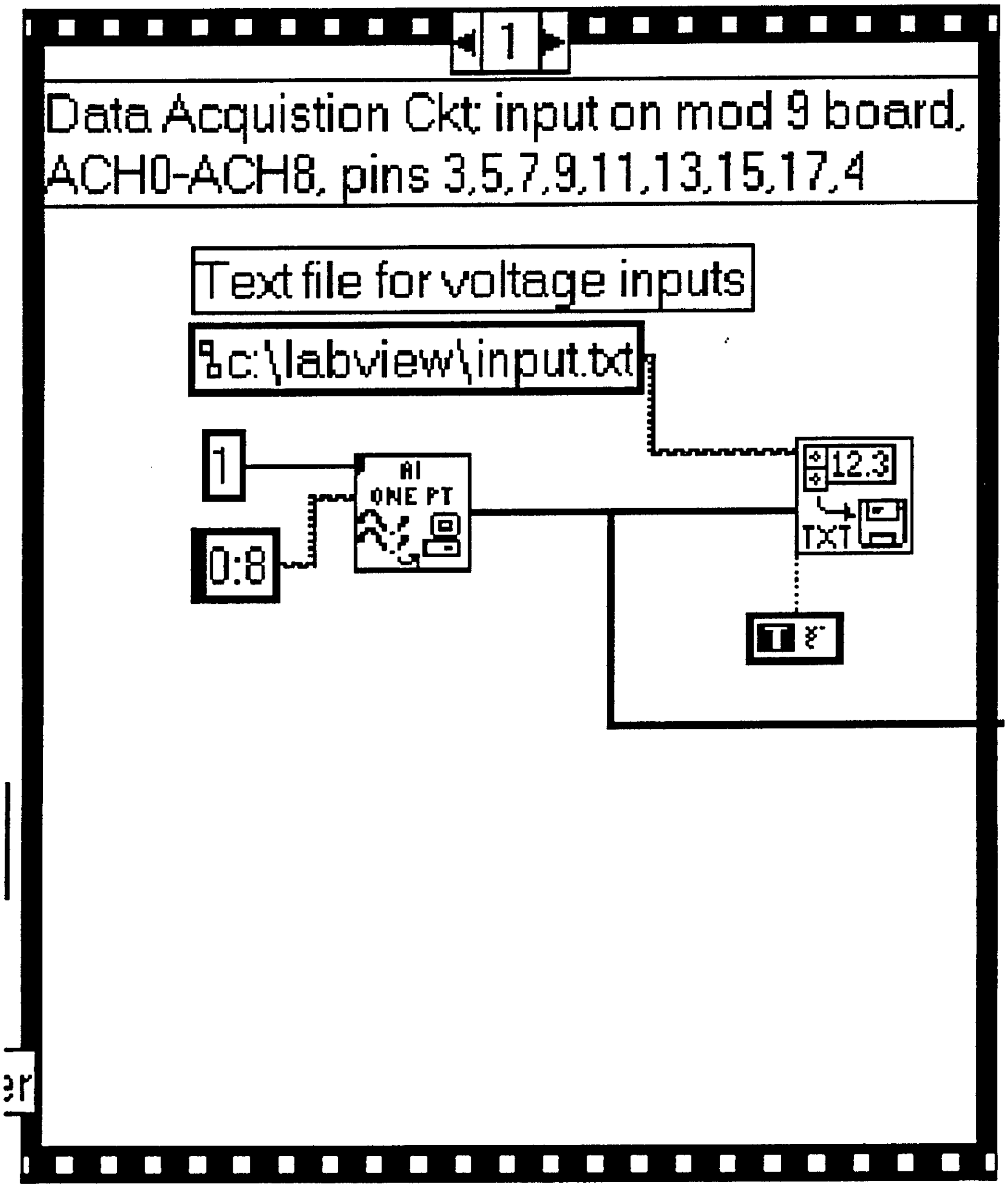


Figure 44. Data Acquisition Sequence "0", CRAIG8.VI



Data Acquistion Ckt: input on mod 9 board, ACH0-ACH8, pins 3,5,7,9,11,13,15,17,4

Text file for voltage inputs

c:\labview\input.txt

Figure 45. Data Acquisition Sequence "1", CRAIG8.VI

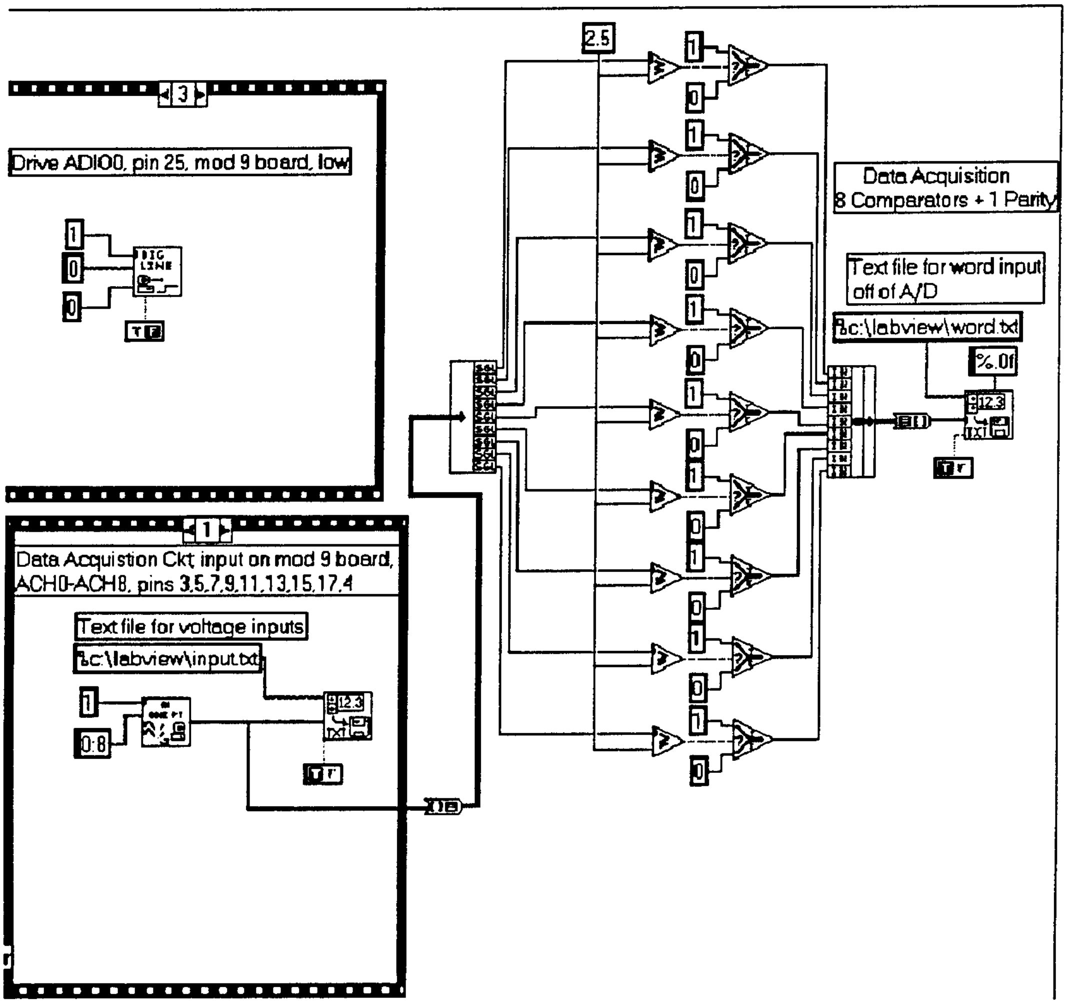

3
Drive ADIO0, pin 25, mod 9 board, low
DIG LINE
1
0
0
1
Data Acquistion Ckt input on mod 9 board, ACH0-ACH8, pins 3,5,7,9,11,13,15,17,4
Text file for voltage inputs
c:\labview\input.txt
1
0:8
12.3
TXT
2.5
1
0
Data Acquisition 8 Comparators + 1 Parity
Text file for word input off of A/D
c:\labview\word.txt
%.0f
12.3
TXT

Figure 46. Simulated Comparator Bank, CRAIG8.VI

APPENDIX B. MATLAB SOURCE CODE

A. ANALYSIS OF LABVIEW VI'S OUTPUTS

The output of the LabVIEW VIs discussed in Chapter II and Appendix A are text files. Matlab is used to analyze and plot these text files. The program MACH1.M is written to plot the characteristic waveforms from the text files MACHOU#.TXT and RAMPIN#.TXT. The program STR.M is written to provide an illustration of a comparator ladder used in Chapter IV. The Matlab source code for MACH1.M and STR.M are given below.

1. MACH1.M

```
% Craig A. Crowe
% Thesis
% Ramp Voltage Out of Labview; Output of Mach-Zhender interferometer
% File: C:\matlab\craig\mach1.m
% Last Revision: 2/28/95


clear

% load data files for analysis

load c:\matlab\craig\machou21.txt
load c:\matlab\craig\rampin21.txt

% Plot MZI #1, M3b, Output Voltage

x1=10*machou21(:,4)-0.0586; % the -0.0586 V is necessary to correct for a 0 V input
```

```
y1=machou21(:,1)-0.0586;  % the -.0586 V is necessary to correct for a 0 V input

plot(x1,y1),title('MZI Transfer Function for NRL MZ # M3b'),xlabel('Input Voltage'),ylabel('Output Voltage')

grid

pause

%  Plot MZI #2, M9c, Output Voltage

x2=10*machou21(:,4)-0.0586;  % the -0.0586 V is necessary to correct for a 0 V input

y2=machou21(:,2)-0.0586;  % the -.0586 V is necessary to correct for a 0 V input

plot(x2,y2),title('MZI Transfer Function for NRL MZ # M9c'),xlabel('Input Voltage'),ylabel('Output Voltage')

grid

pause

%  Plot MZI #3, M8b, Output Voltage

x3=10*machou21(:,4)-0.0586;  % the -0.0586 V is necessary to correct for a 0 V input
y3=machou21(:,3)-0.0586;  % the -.0586 V is necessary to correct for a 0 V input
```

```
plot(x3,y3),title('MZI Transfer Function for NRL MZ # M8b'),xlabel('Input Voltage'),ylabel('Output Voltage')

grid

pause

% Plot Labview Ramp Voltage supplied to Amplifier then to MZI

b=length(rampin21(:,1));

f=1:b;

g=rampin21(:,1);

plot(f,g),title('Ramp Input Voltage to MZI Out of LabVIEW'),xlabel('Index Point'),ylabel('Voltage')

grid
```

2. STR.M

```
% This file produces a staircase output
% Craig A. Crowe
% Filename: str.m
% last revision 3/9/95

clear
```

```
a=1:15;

b=-1.875:250e-3:1.625;

stairs(b,a), xlabel('Volts'), ylabel('Step Number')

grid

pause

%  This part of the program prints the Normalized Output Voltage of an Interferometer from
%  -Vmax to +Vmax ie., -31.875V to +31.875V.

v=-31.875:62.5e-3:31.875;

y=0.5+0.5*cos(v*1.4+pi);

plot(v,y), xlabel('RF Input Voltage'), ylabel('Normalized Output Amplitude'), title('Ideal Folded Output Waveform');

grid
```

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